FUNCTION AND CONSTRUCTION OF COAXIAL CONNECTORS, AND THE GOLDEN RULES OF THEIR USE IN PCB DESIGN

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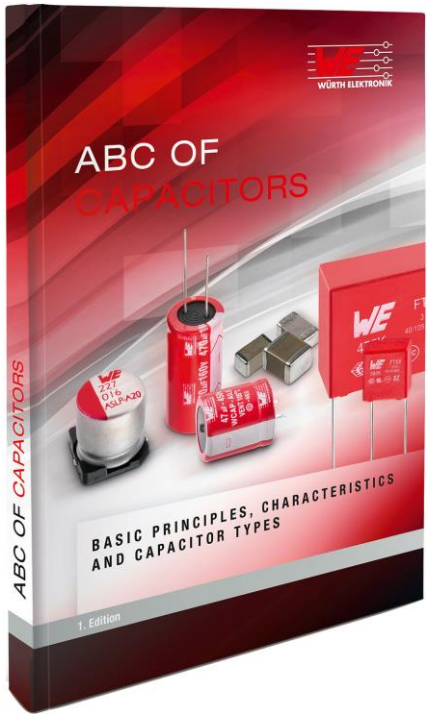
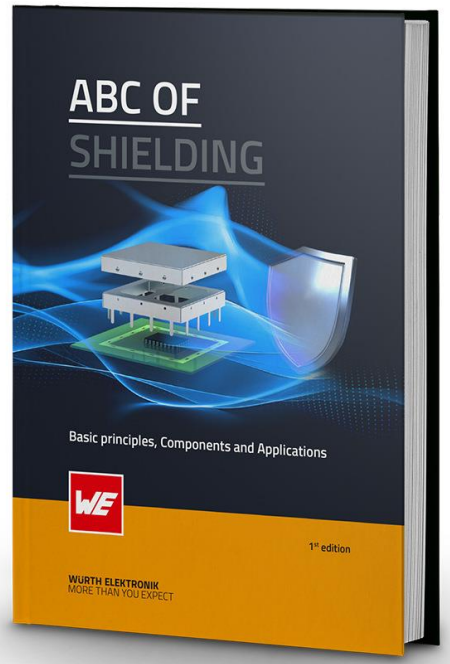
TRILOGY OF
CONNECTORS
Basic principles and connector design explanations
4th extended and revised edition
WÜRTH ELEKTRONIK
MORE THAN YOU EXPECT


WÜRTH ELEKTRONIK
ABC OF
CAPACITORS
BASIC PRINCIPLES, CHARACTERISTICS
AND CAPACITOR TYPES
ABC OF CAPACITORS
1. Edition


ABC OF
SHIELDING
Basic principles, Components and Applications
1st edition
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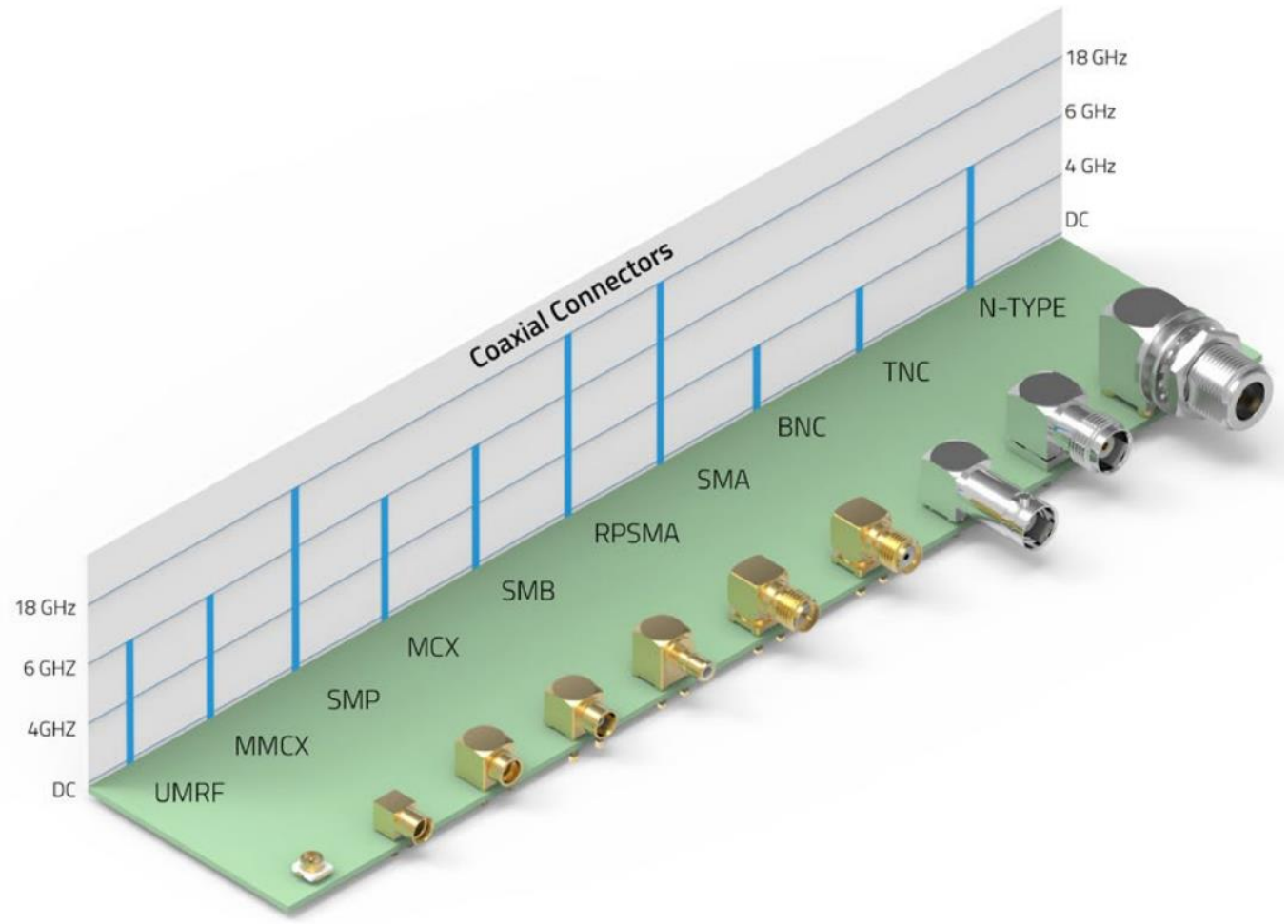
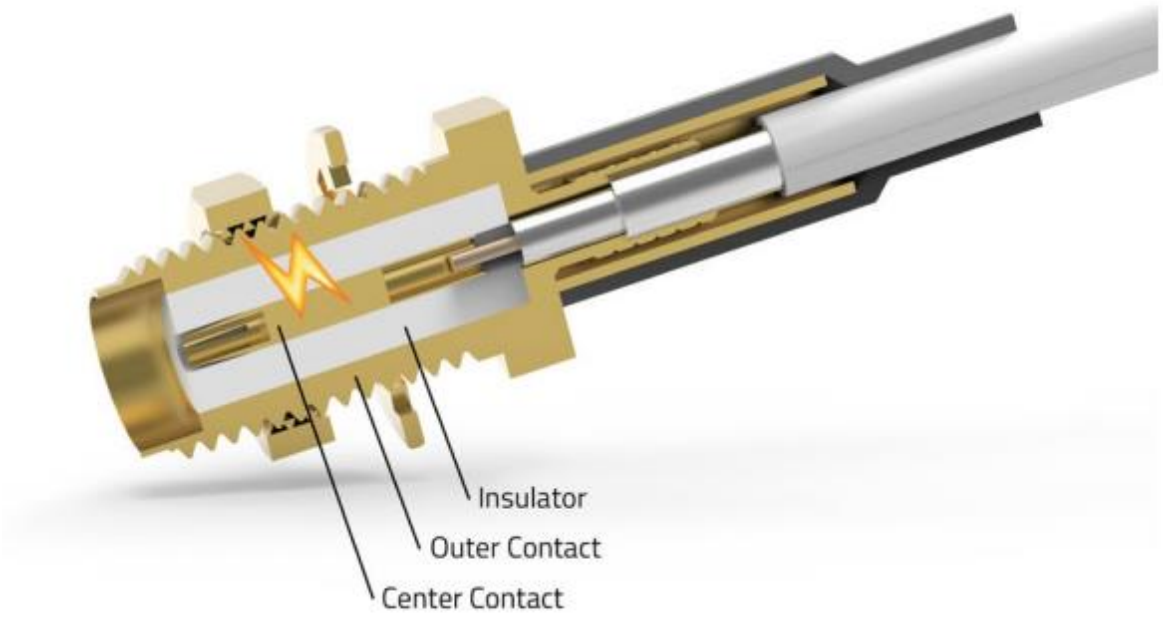
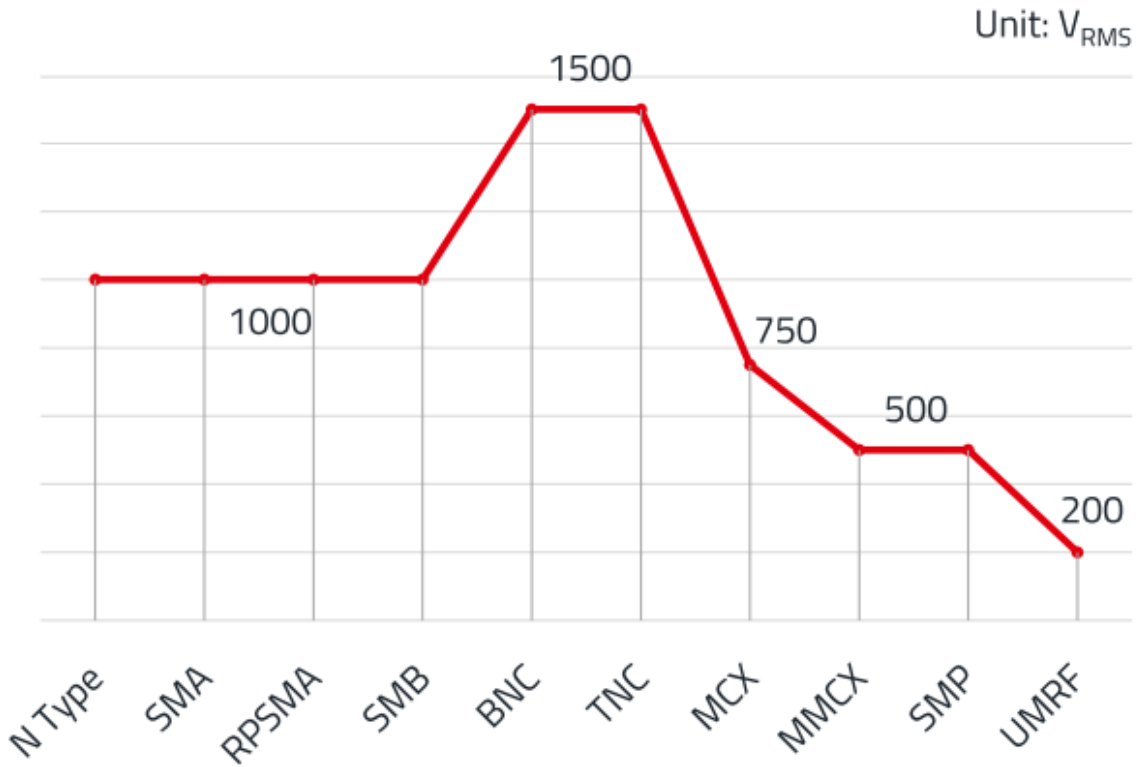
MORE THAN YOU EXPECT

COAXIAL CONNECTORS

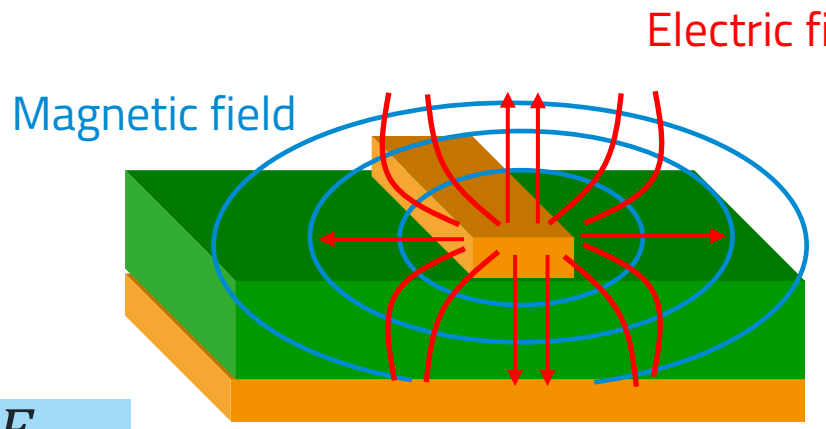


VOLTAGE HANDLING



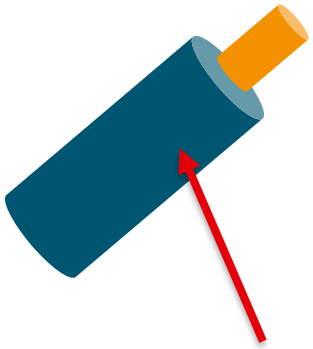


PERMITTIVITY



$$Z_C = \frac{E}{H}$$

$$Z_c = \sqrt{\frac{\mu_0 \cdot \mu_r}{\varepsilon_0 \cdot \varepsilon_r}}$$



ε_0 : vacuum electrical permittivity (**Fm^{-1}**)

ε_r **:** dielectric relative permittivity

Material	Relative permittivity ε_r
Vacuum	1
Air	≈1
PTFE (Teflon)	2.1
PET	2.3
Roger (RO4003)	3.6
FR4	4.5
PVC	5
glass	≈5 to 7.5
water	≈80 (at 20°C)

PCB CONNECTORS

- Fixed PCB thickness
- Flat tab & round post pin

End launch

Through hole

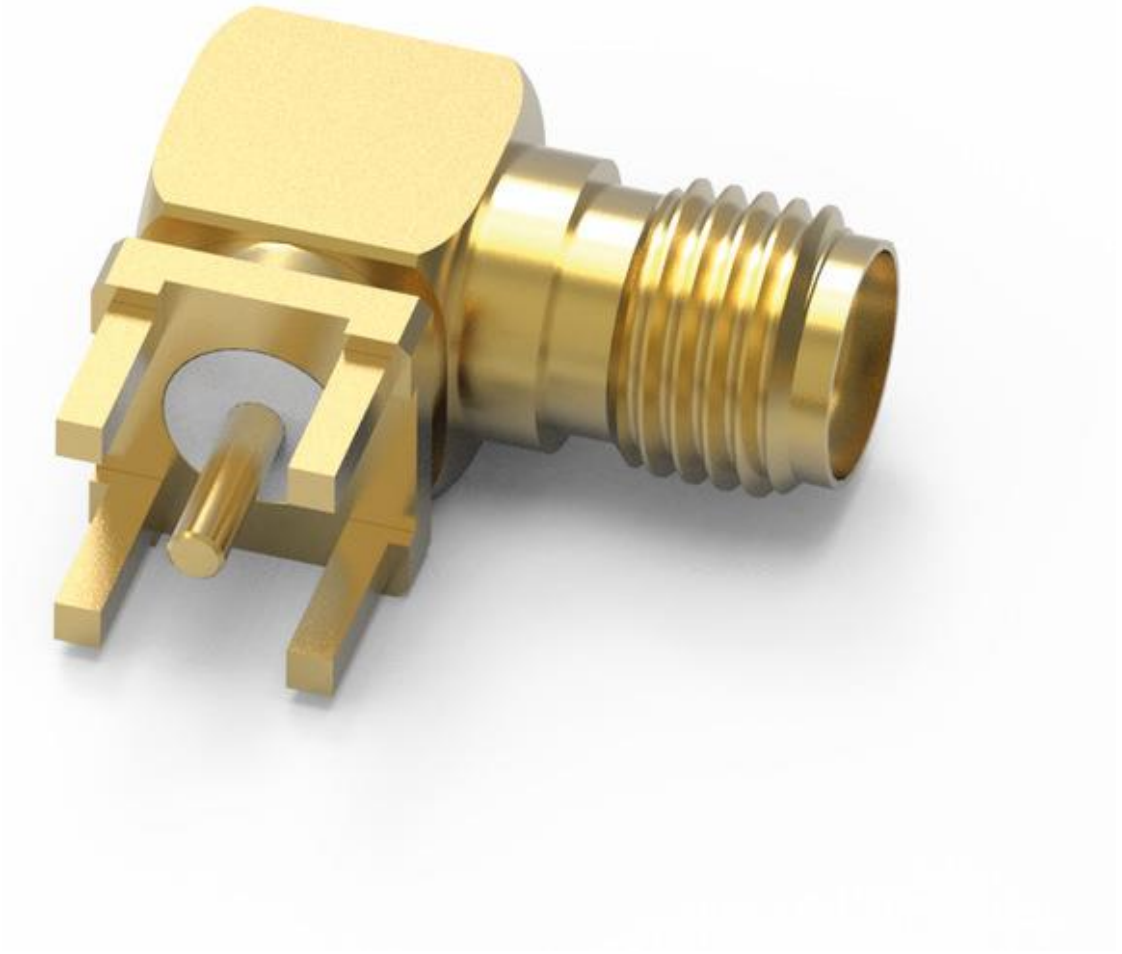
- Good retention on PCB
- Wider range of PCB thickness
- Available with SMT & THR signal pin

- Full SMT
- PCB edge card

Surface mount

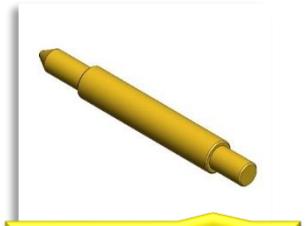
Surface mount

- Full SMT



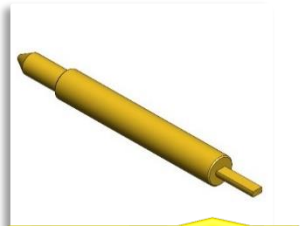
PCB CONNECTORS

Center contact back shape



Round post

- Good contact
- Low frequency



Flat tab

- Easy PCB design
- High frequency

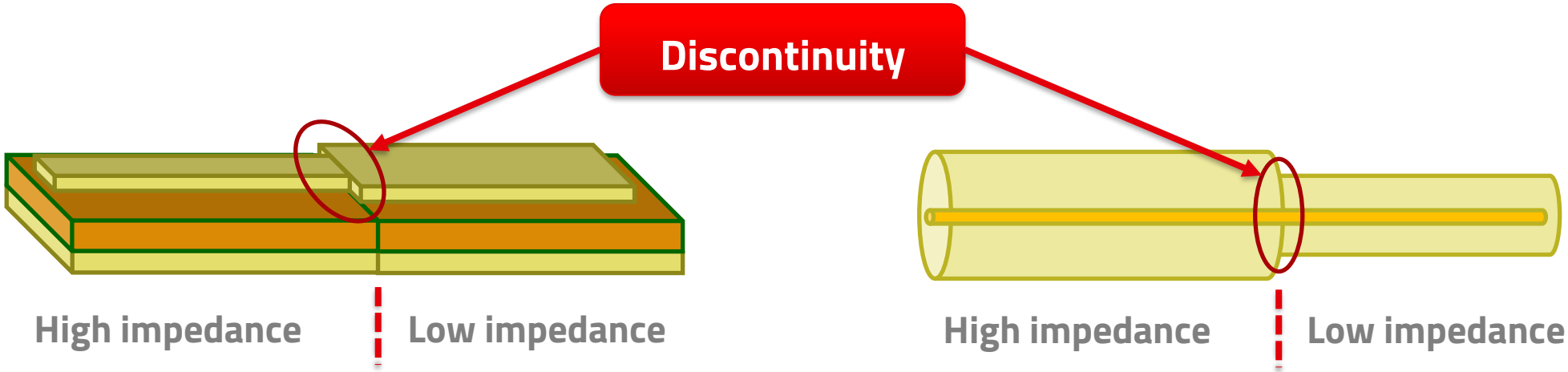
PCB thickness

1.1mm & 1.6mm

Up to 2.8mm

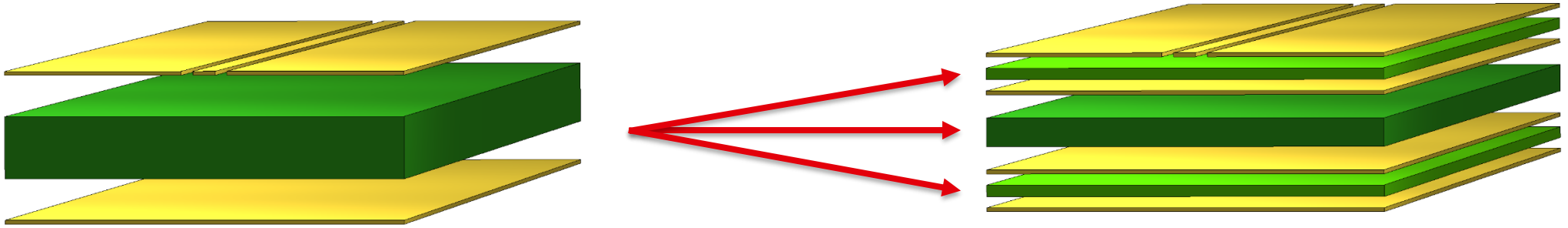
DISCONTINUITY IMPACT

- **Impedance variation on RF-path**



- **Causes:**
  - Reflection
  - Field conversion

TYPICAL LAYER SETUP

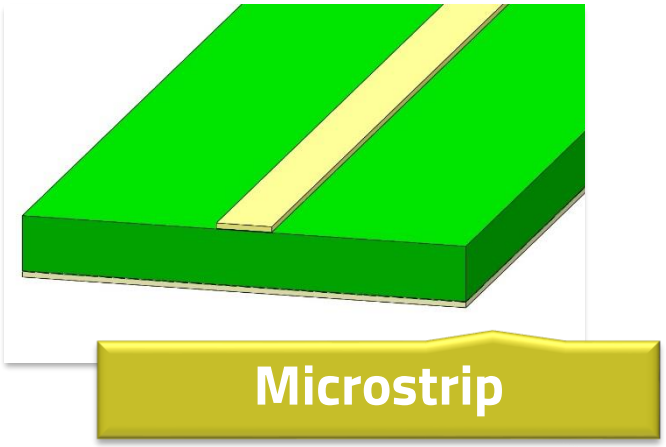


2-Layer	
Height	1.55 mm
Prepreg + core	FR4

4-Layer	
Height	1.55 mm
Prepreg + core	FR4

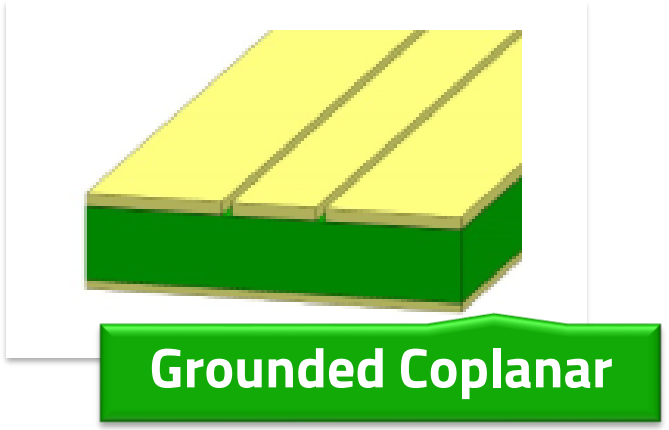
- **Low production cost**
  - Mostly no separate GND-Plane
- **Good for RF-Designs**
  - Separate GND-Plane
  - Dielectric differs

PLANAR TRANSMISSION LINES



- Wider line width
- Antenna fed-line
- No Ground on RF-Layer

- Line width depends on substrate height and ε_r



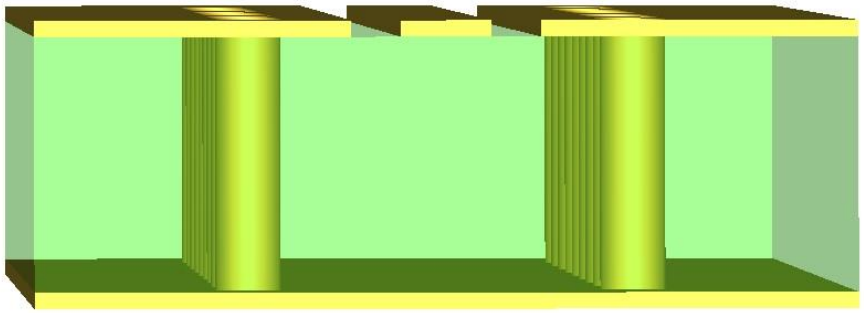
- Smaller line width
- Ground connection to components
- Various planar matching designs

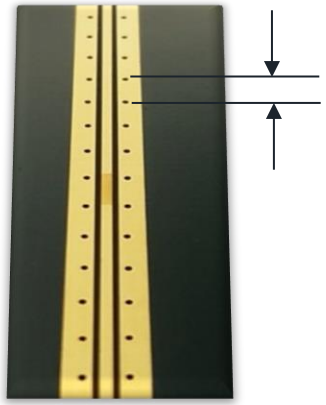
- Line width depends on substrate height. ε_r and gap width

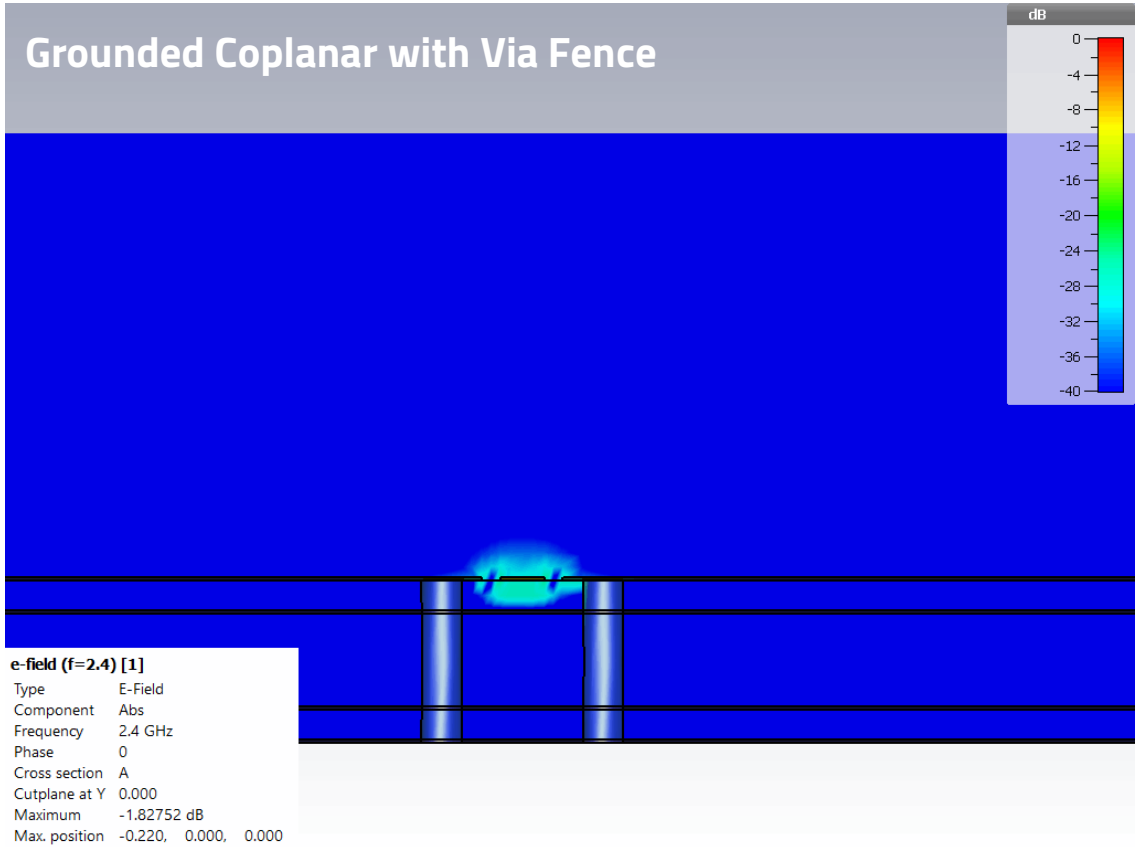
OVERVIEW PCB STRUCTURES: TIPS & TRICKS

VIA FENCE

Via center distance ~ λ/10



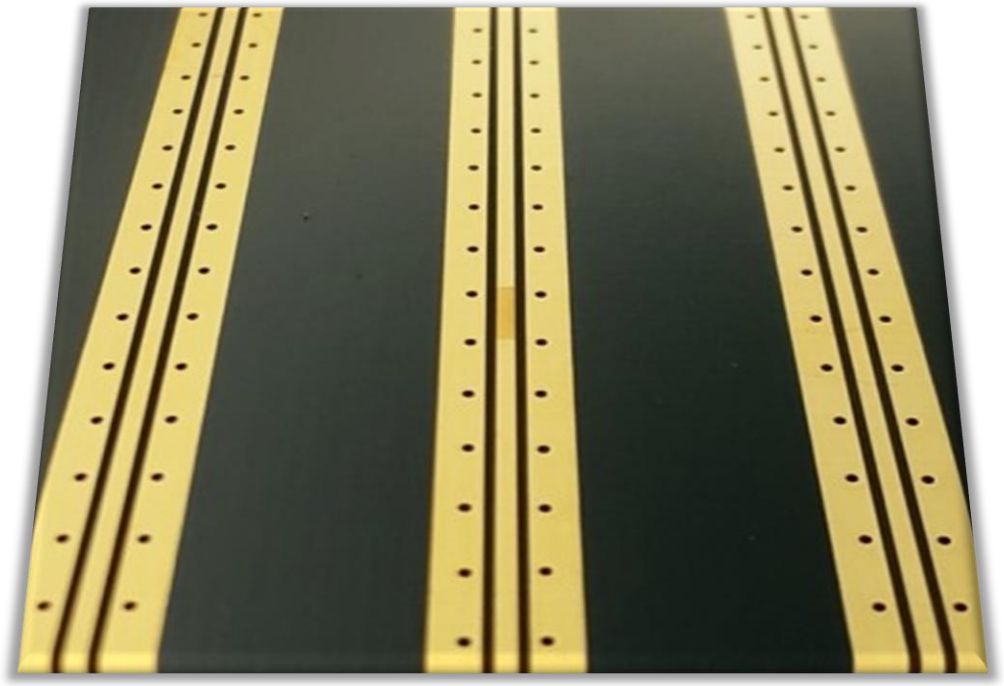




- **Field captured between GND**
  - Reduces coupling
  - Less loss
- **Stabilized ground planes**

OVERVIEW PCB STRUCTURES: TIPS & TRICKS

SOLDER-RESIST FREE

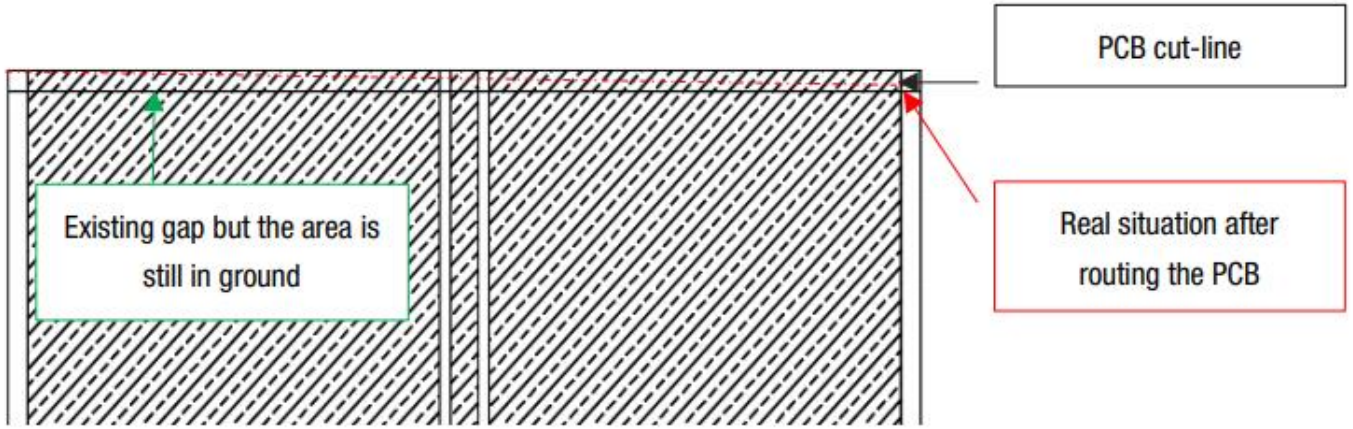


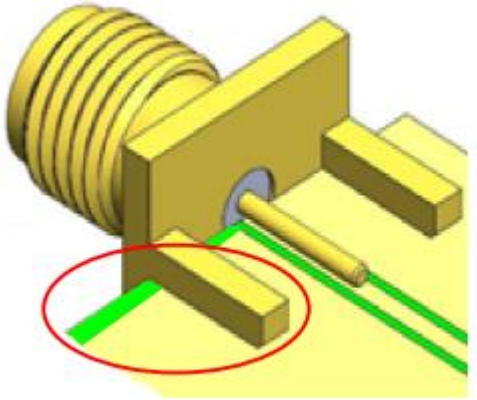
- **Solder resist:**
  - Increases loss
  - Adds dielectric
- **Remove solder resist from:**
  - RF-Line and
  - Near Ground-Plane

COMBINATION CONNECTOR & PCB: EXAMPLES

CPWG - ROUND: DESIGN - DGS

- **PCB edge**

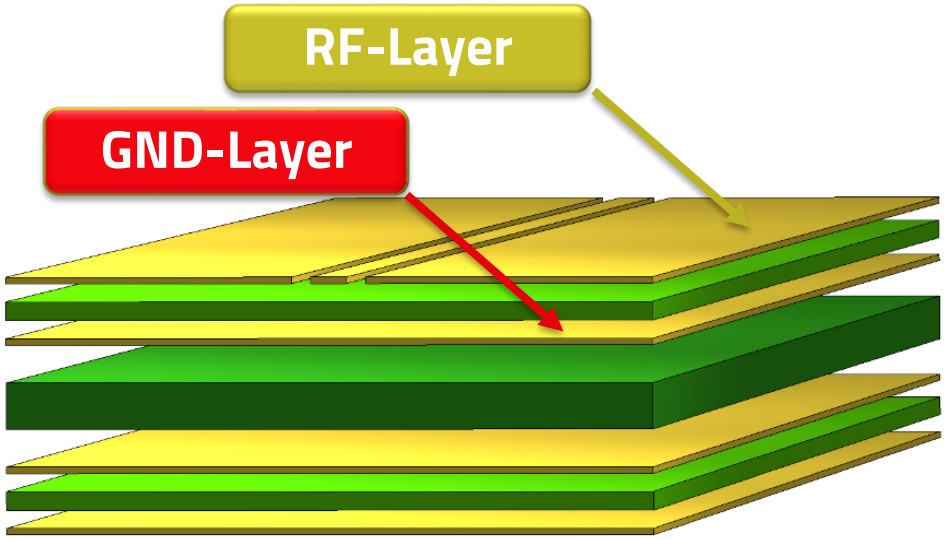




After soldering the connector, a gap exist without ground

OVERVIEW PCB STRUCTURES: TIPS & TRICKS

LAYERS

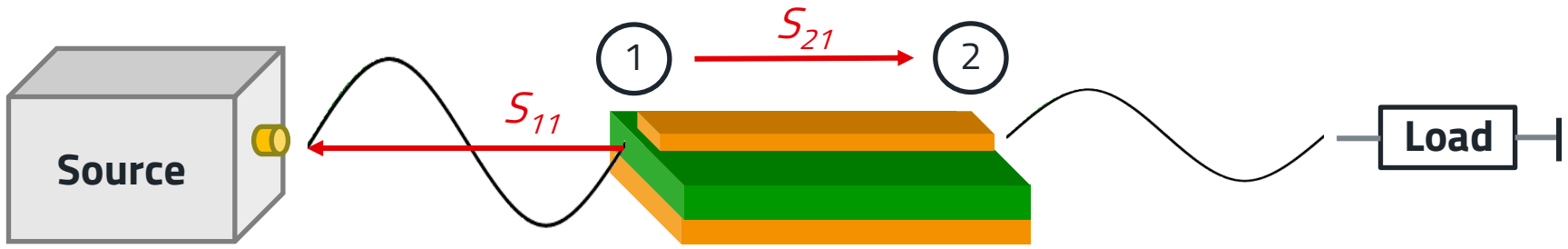


- **Top or Bottom as RF-Layer**
  - Reduced loss
  - No Vias inside trace → Mismatch!
- **Seperate ground-layer underneath RF**
  - Decreases discontinuities
  - Good connection to RF-Layer GND needed!

S PARAMETERS

$$S_{ji} = 10 \log \frac{power\ j}{power\ i} \text{(dB)}$$

- **Factor of reflection and throughput:**



- **S-Matrix:**
  - S_{ii}: Reflection at Port i
  - S_{ji}: Insertion losses from Port i to Port j
- **Power domain!**

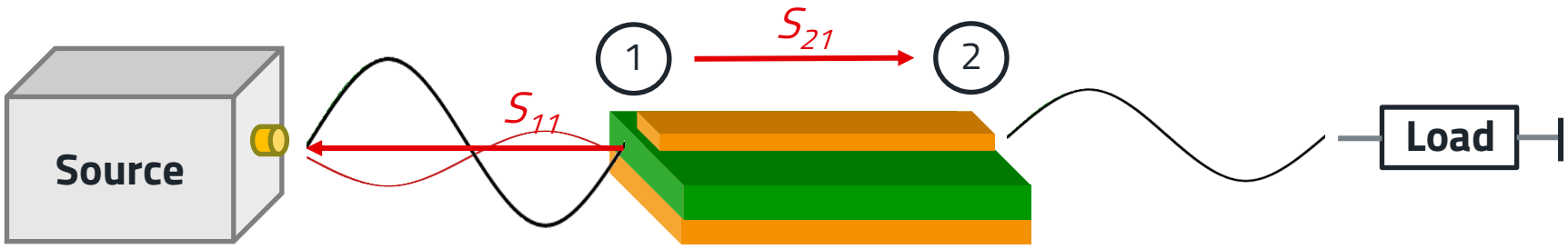
- **Mostly given in dB:**
  - e. g. $-3dB = 10 \times \log(0.5)$

Signal power-50%

- **Calculation from source:**
  - $1000\ mW \times 0.5 = 500mW$
  - $30dBm - 3dB = 27dBm$

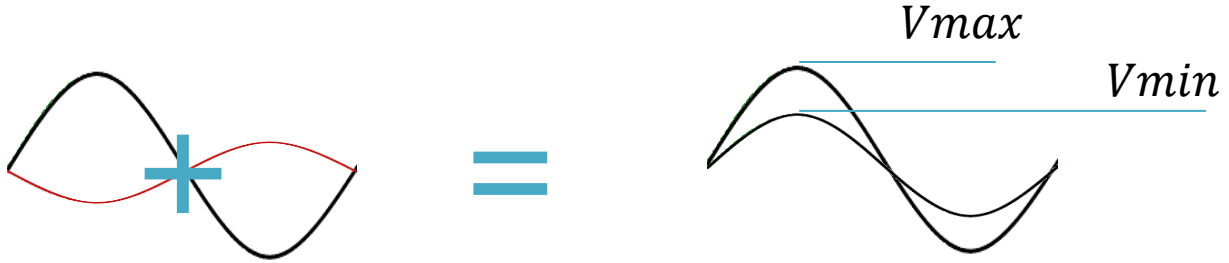
S PARAMETERS: VSWR

- **Voltage standing wave ratio (VSWR):**



- **Only reflection/return loss:**

$$VSWR = \frac{Vmax}{Vmin}\ [dB]$$



- **Voltage domain!**

S PARAMETERS & VSWR

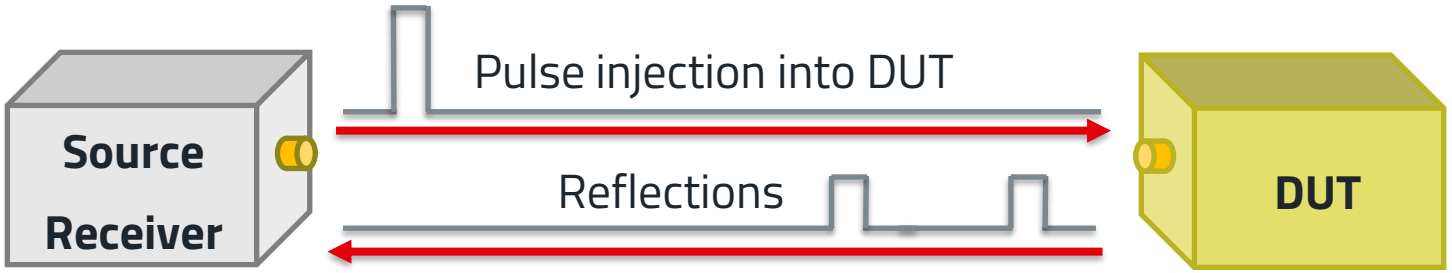
VSWR	Return Loss (dB)	Reflection (%)	
1.0	∞	0	Very well matched
1.02	40.1	0.01	
1.03	35.3	0.03	
1.1	26.4	0.23	Well matched
1.12	24.9	0.32	
1.15	23.1	0.49	
1.2	20.8	0.83	Matched
1.3	17.7	1.70	
1.4	15.6	2.75	
1.5	14.0	3.98	Poorly matched
1.7	11.7	6.76	
1.8	10.9	8.13	
2.0	9.5	11.22	Not matched

$$S_{11} = 10 \log \frac{power\ sent\ 1}{power\ received\ 1} (\text{dB})$$

- **Return loss example:**
  - 20 dB: 99 % insertion & 1% reflection
  - 15 dB: 97% insertion & 3% reflection
  - 10 dB: 90% insertion & 10% reflection
  - 6 dB: 75% insertion & 25% reflection

TIME DOMAIN REFLECTOMETRY

- **Wave impedance measurement through a system**

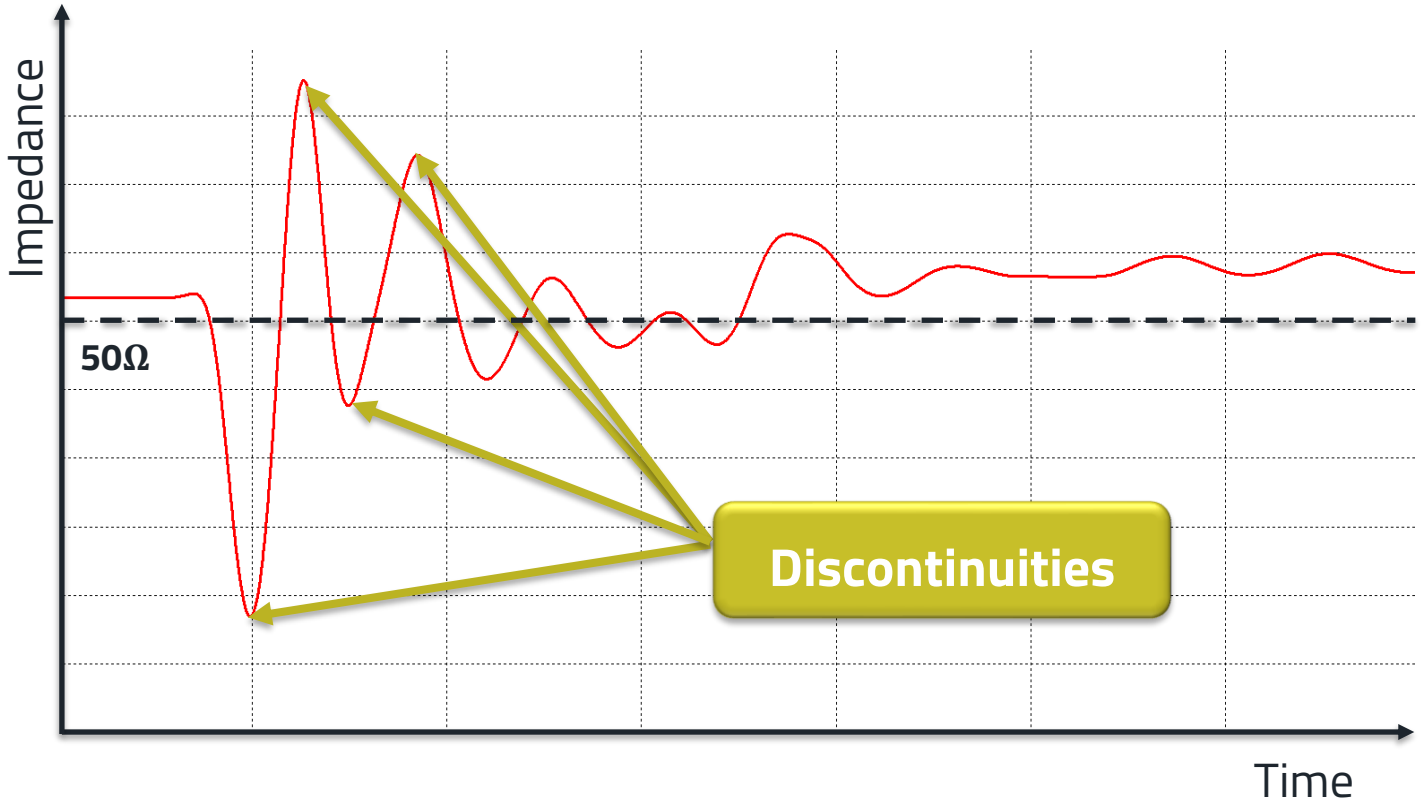


- **Measurement of reflections**
  - Amplitude
  - Time

VNA calculation

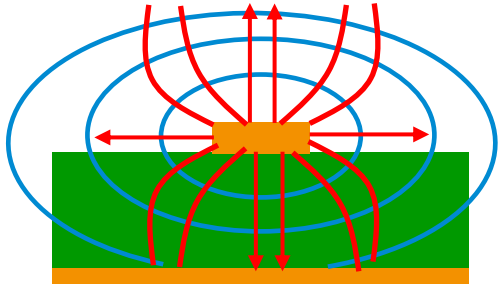
- **Characteristic impedance**

TIME DOMAIN REFLECTOMETRY

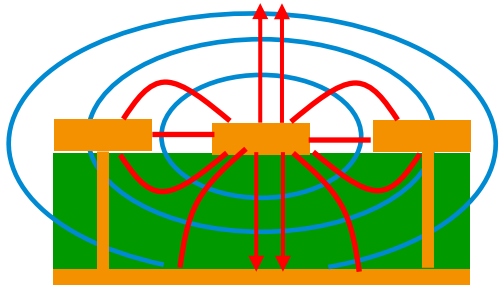


- **Time ~ Length :** $\mathbf{L} = \frac{c}{\sqrt{\varepsilon_r \mu_r}} \times t$

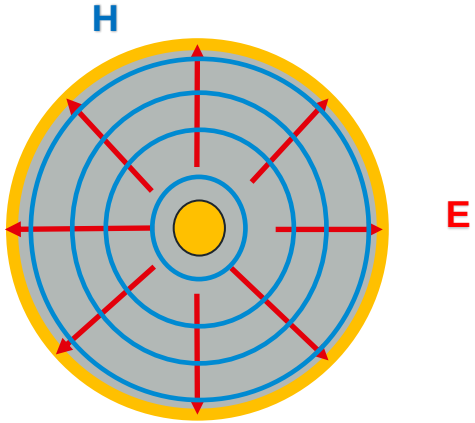
RADIATION - WAVE GUIDE LOSSES



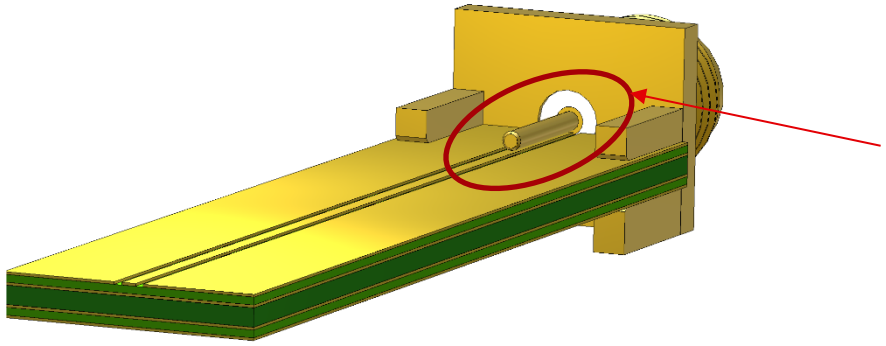
Microstrip : middle losses



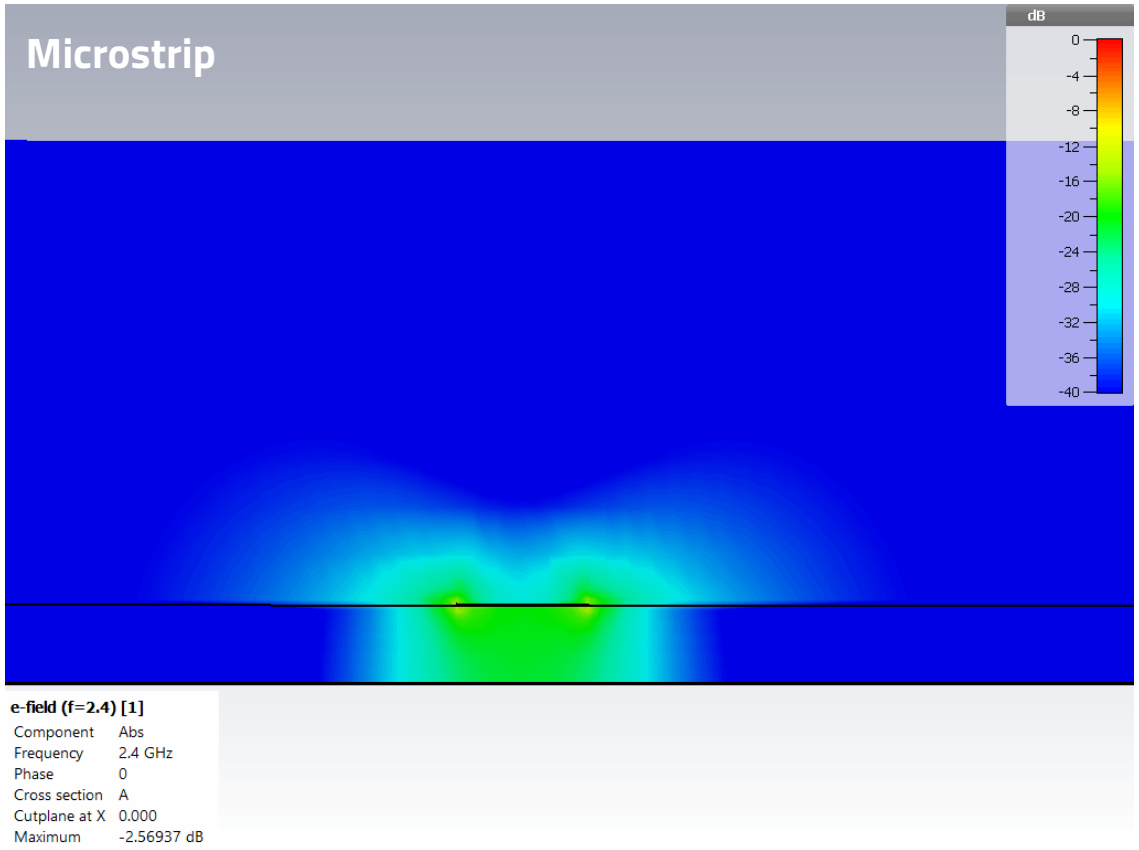
Ground coplanar: low losses

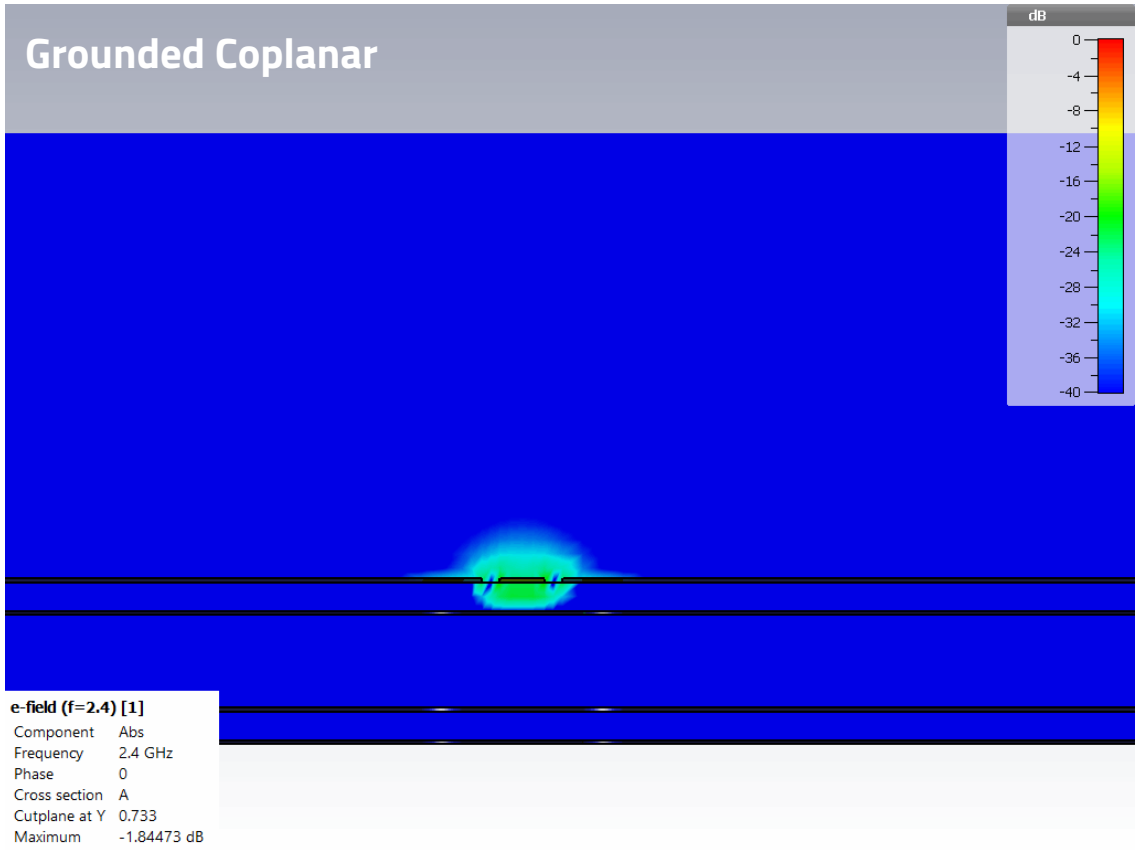


Coax: very low losses



FIELD DISTRIBUTION

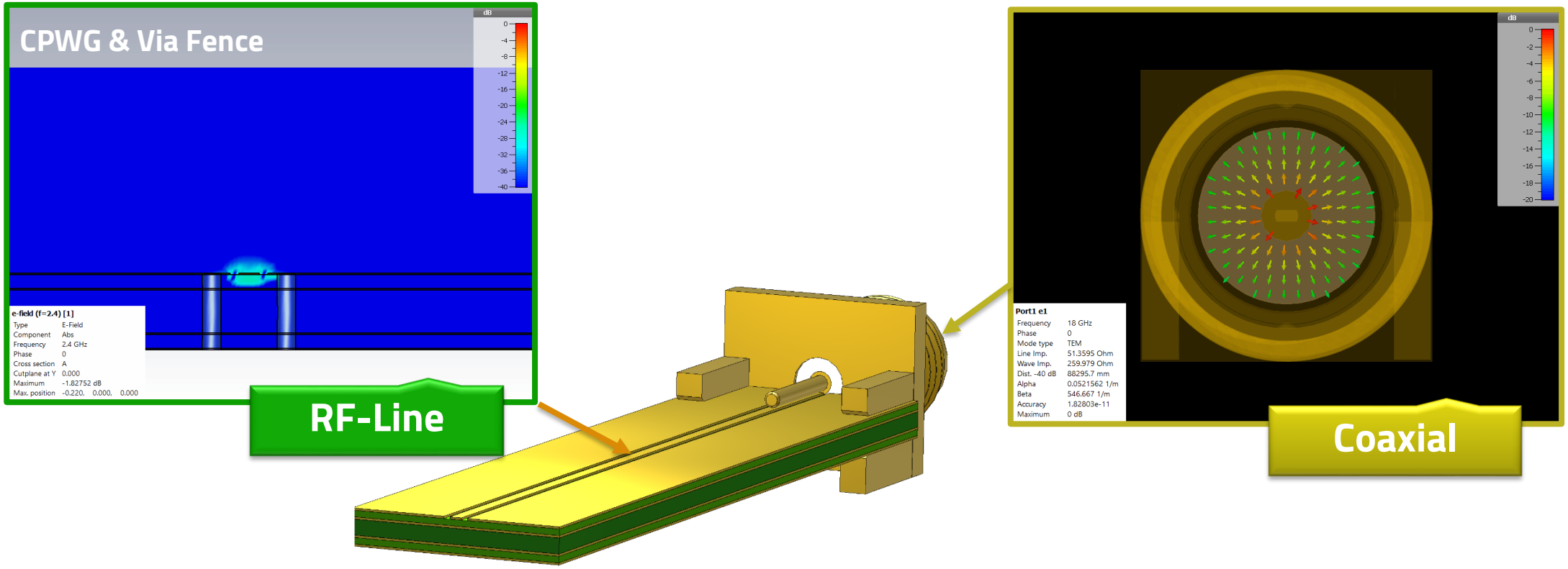




COMBINATION CONNECTOR & PCB: RF-EFFECTS

FIELD CONVERSION (1)

- **Geometry of field changes at connection point**



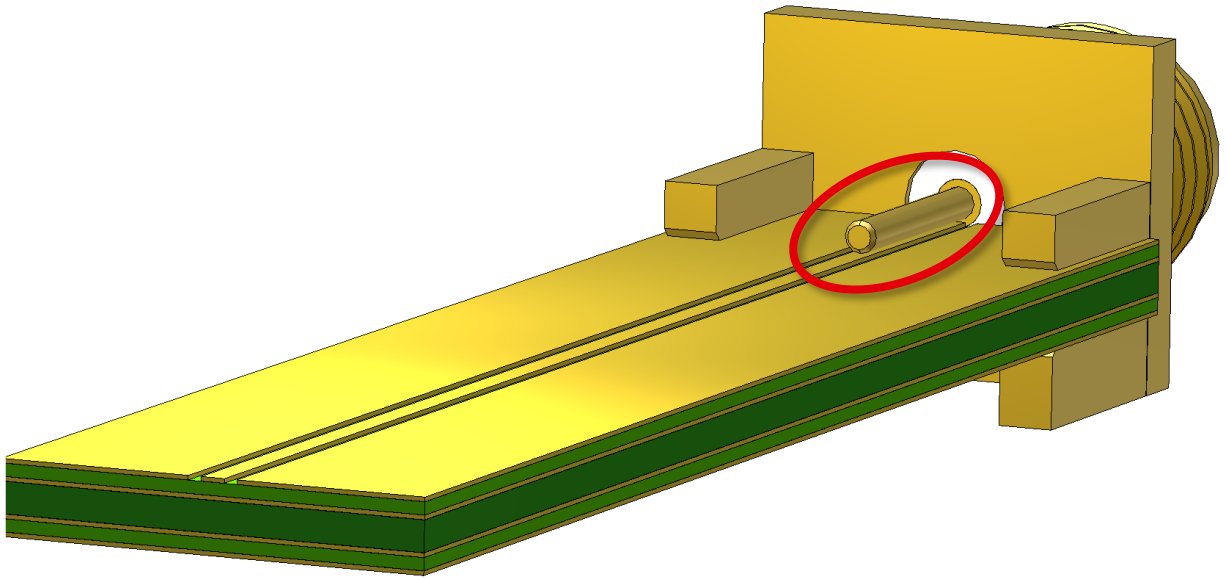
COMBINATION CONNECTOR & PCB: RF-EFFECTS

DISCONTINUITIES

- **Discontinuity at connection point**
  - Change in line impedance
  - Field conversion

- **Huge Mismatch and Reflection!**

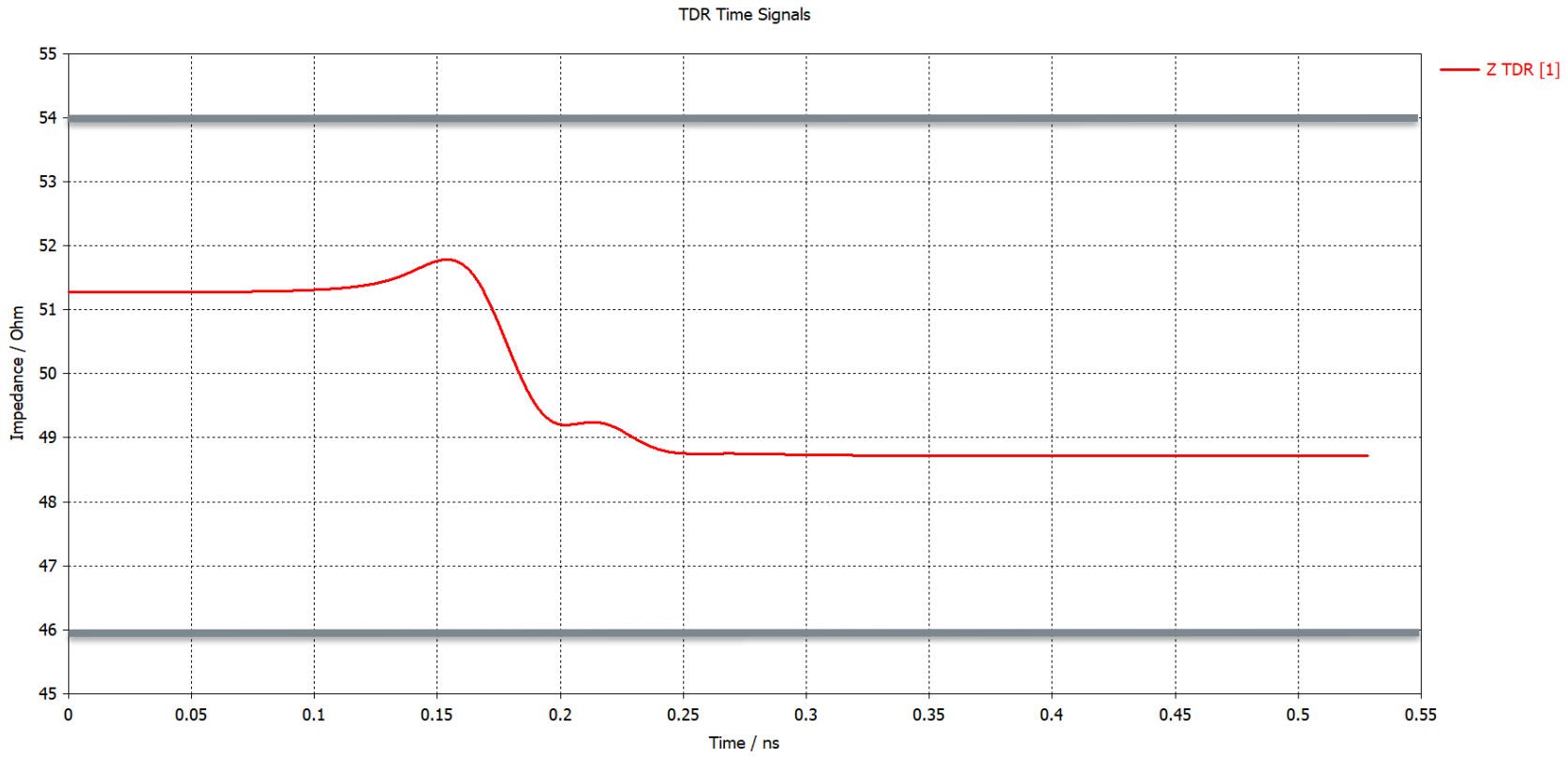
- **Planar matching circuit needed**



COMBINATION CONNECTOR & PCB: EXAMPLES

PROPERTIES

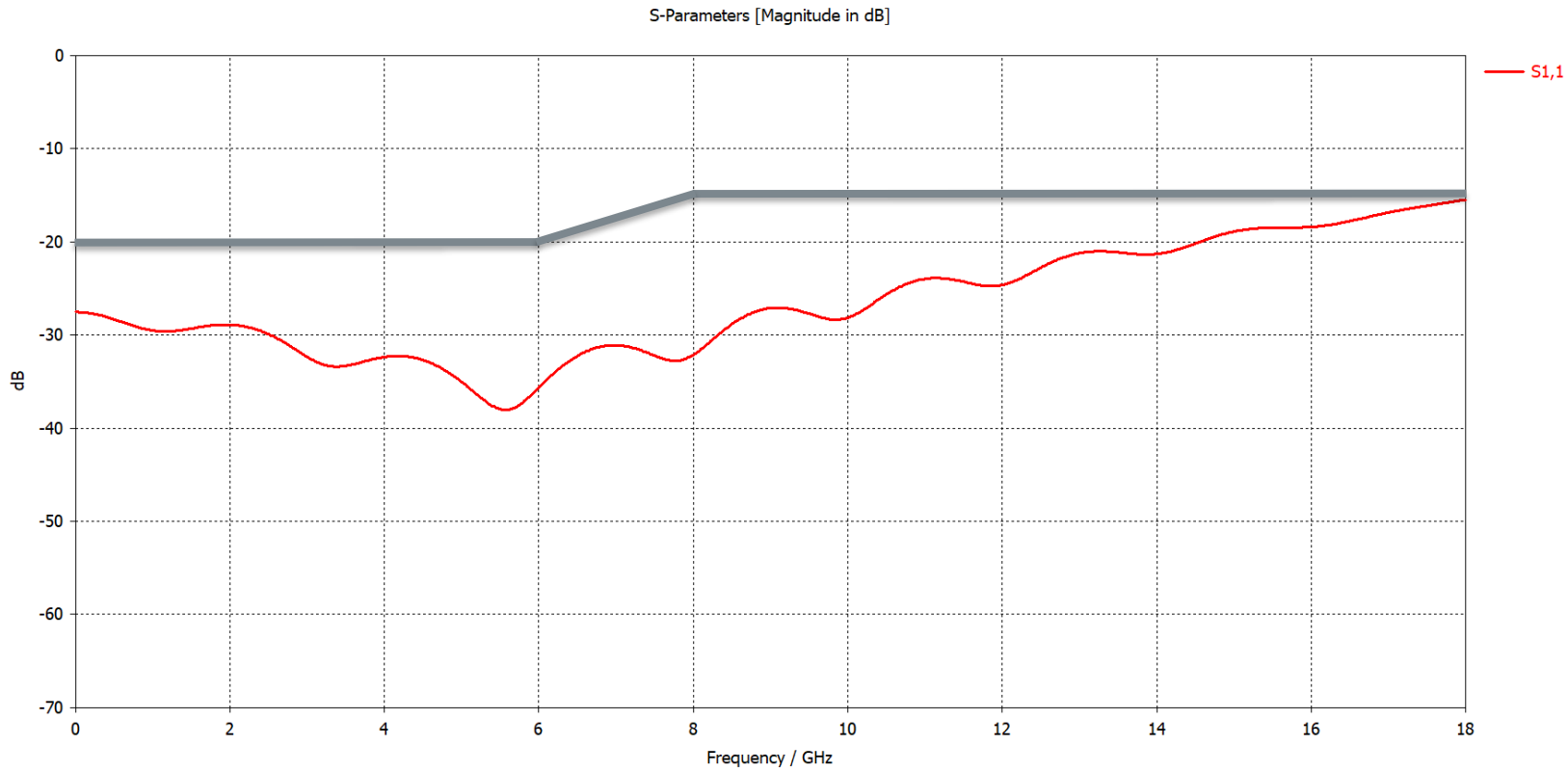
Characteristic impedance limits



COMBINATION CONNECTOR & PCB: EXAMPLES

PROPERTIES

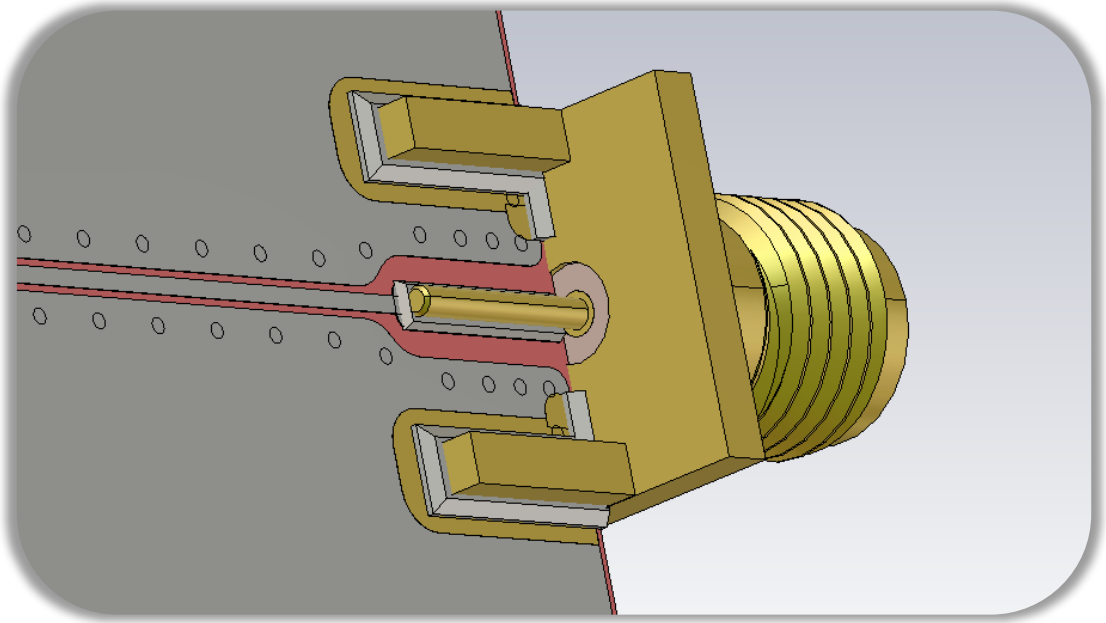
Return loss S11 limits

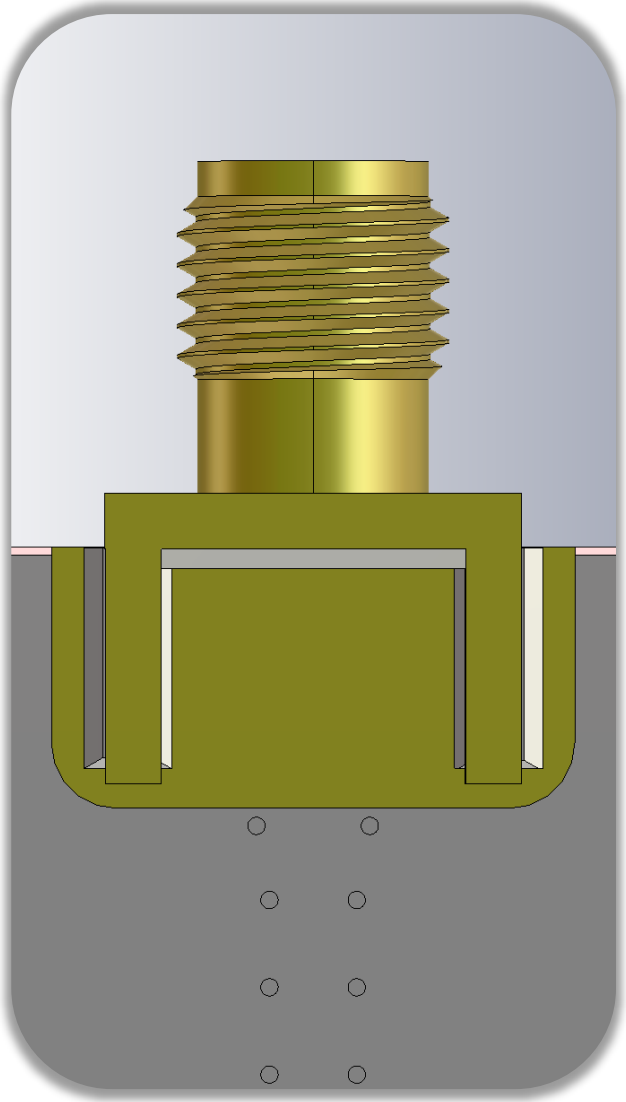


COMBINATION CONNECTOR & PCB: EXAMPLES

CPWG - ROUND: DESIGN

- Solder pads & several vias
- Very good GND connection
- Optimized RF-Line with tapers





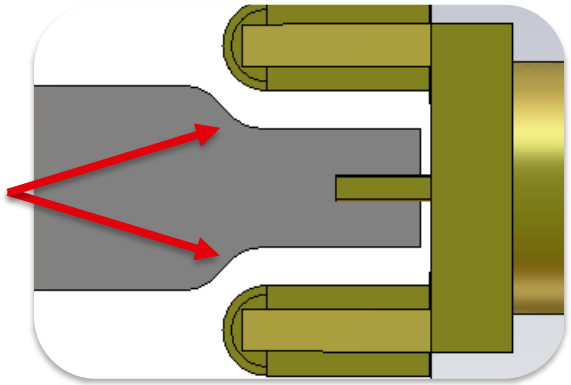
OVERVIEW PCB STRUCTURES: TIPS & TRICKS

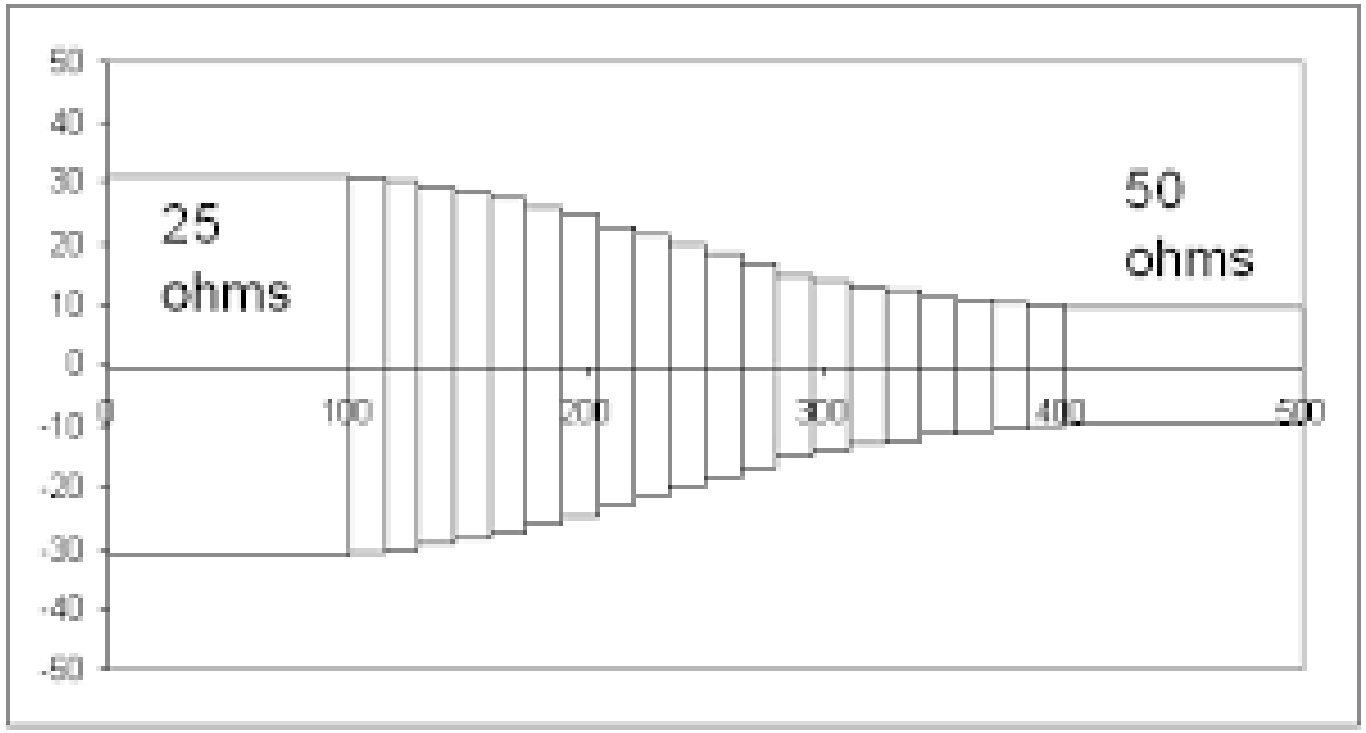
PLANAR IMPEDANCE MATCHING

Taper Structures

Background information

Line Taper

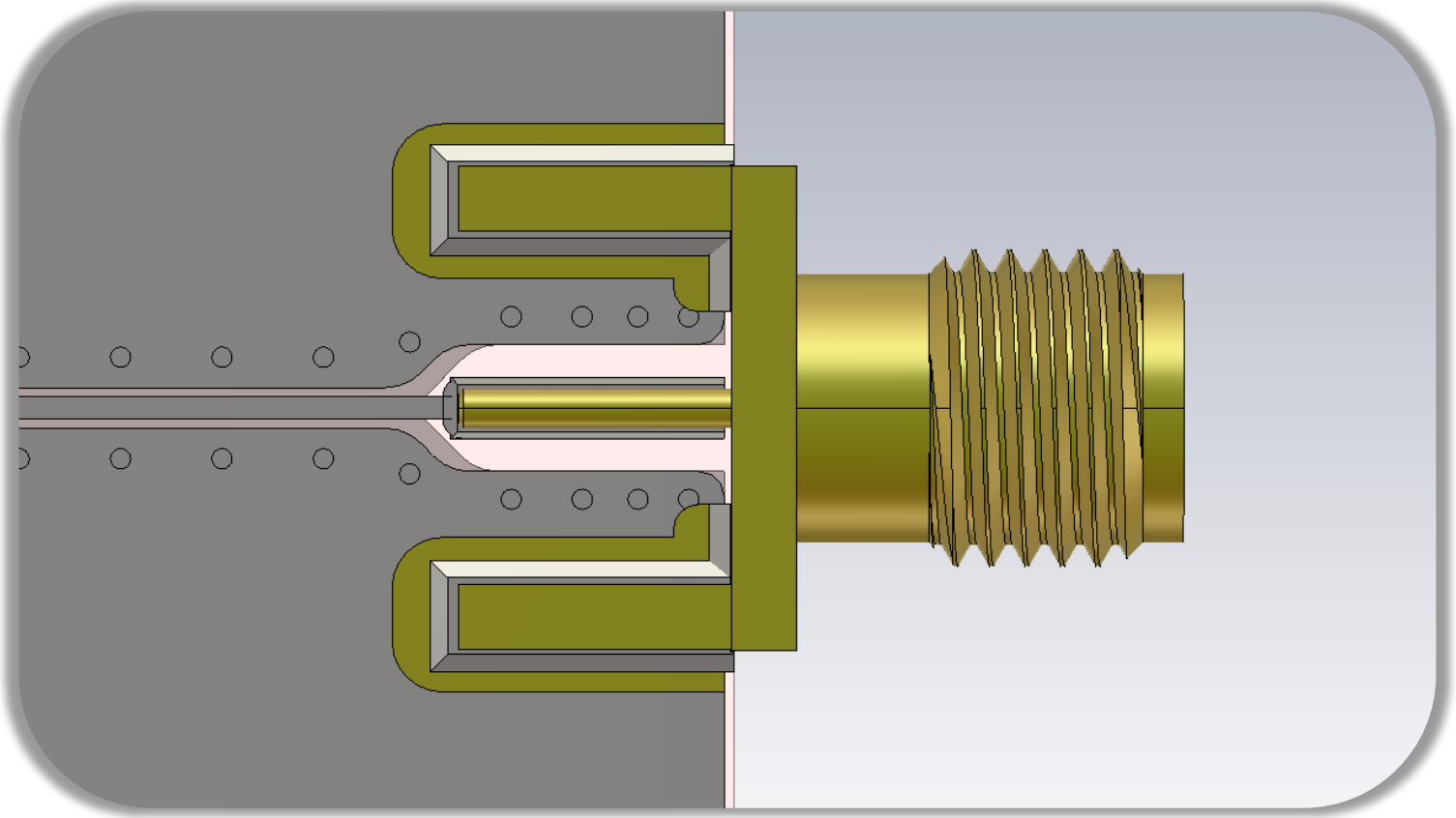




COMBINATION CONNECTOR & PCB: EXAMPLES

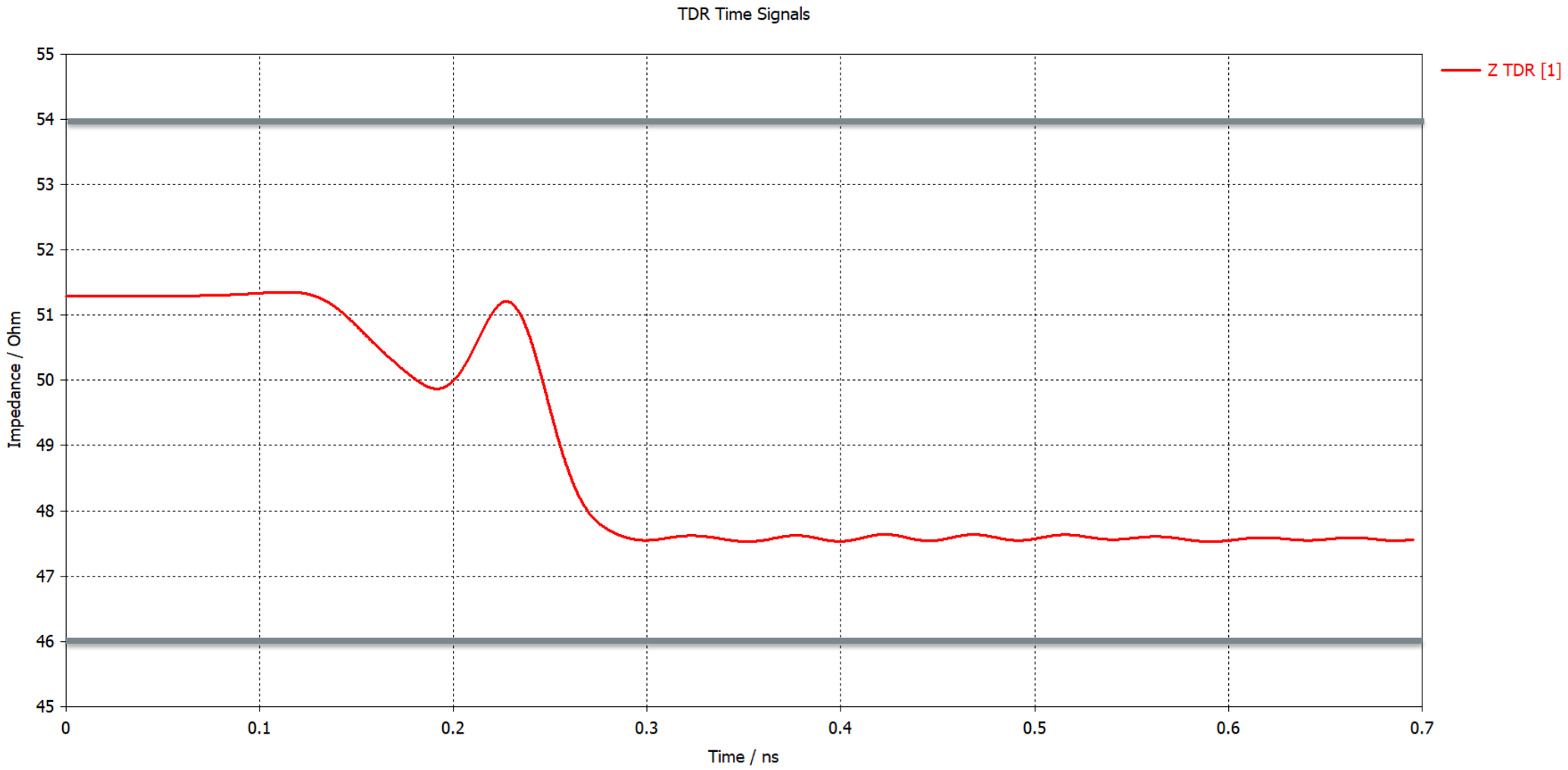
CPWG - ROUND: DESIGN - DGS

- Defective Ground Structure: matching structure → decreases parasitic capacitance



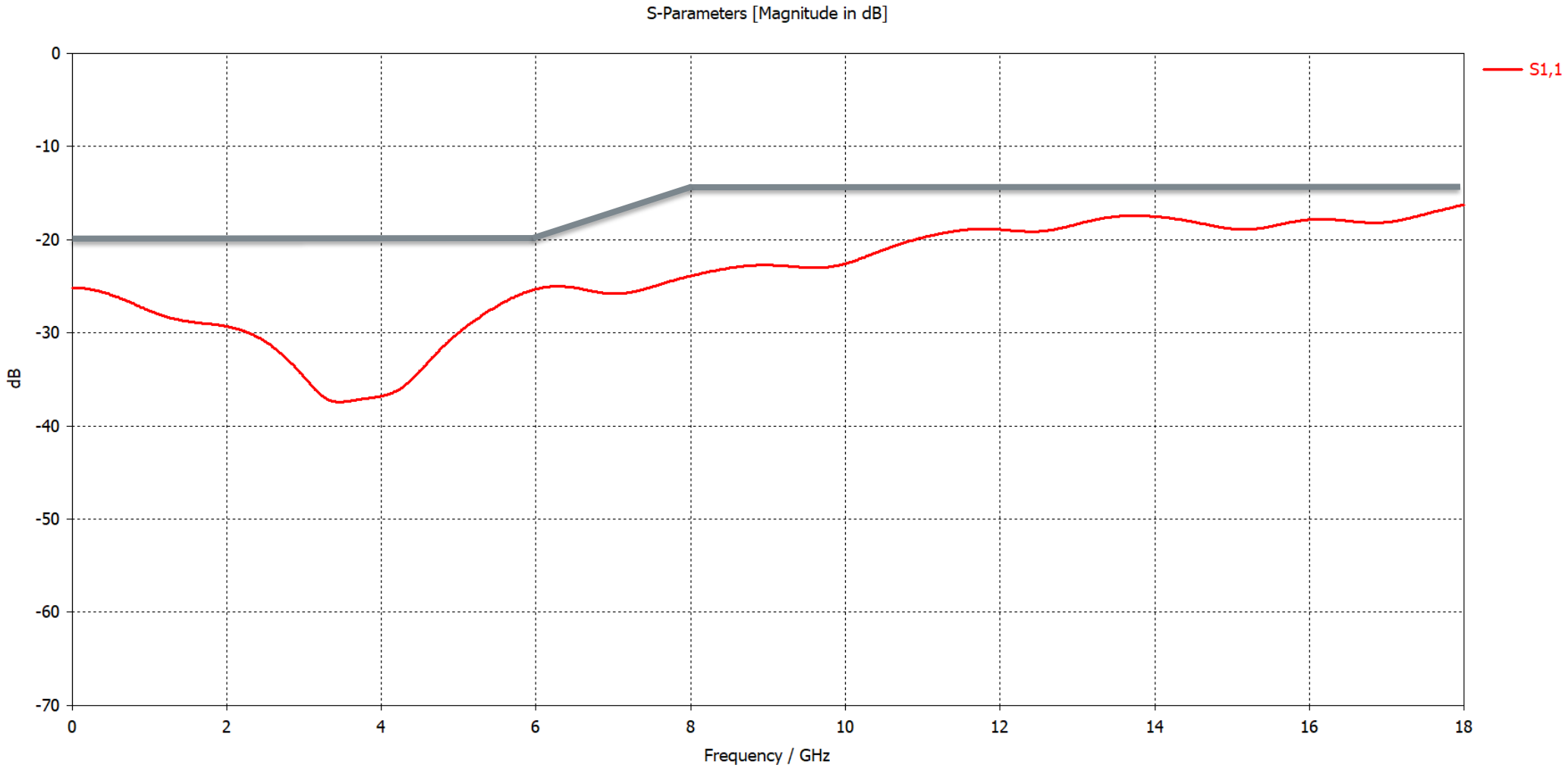
COMBINATION CONNECTOR & PCB: EXAMPLES

CPWG - ROUND: TDR



COMBINATION CONNECTOR & PCB: EXAMPLES

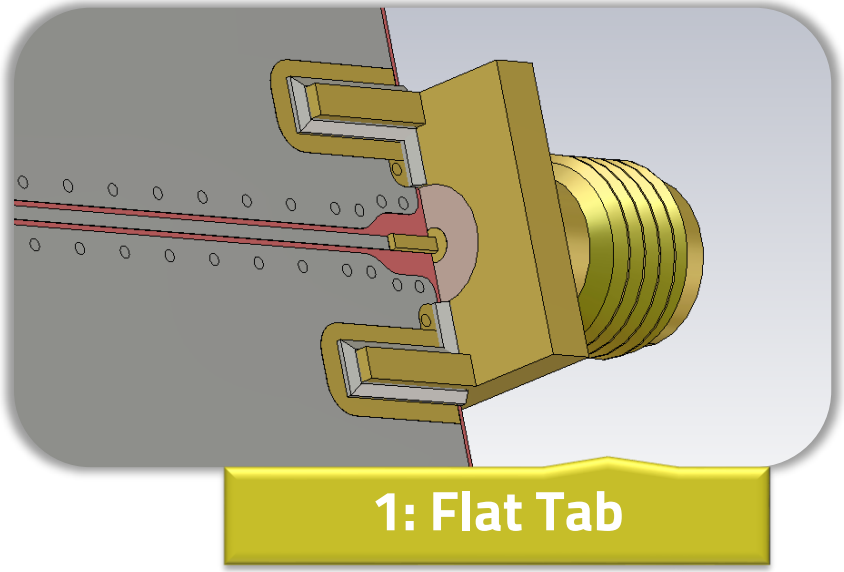
CPWG - ROUND: S-PARAMETER



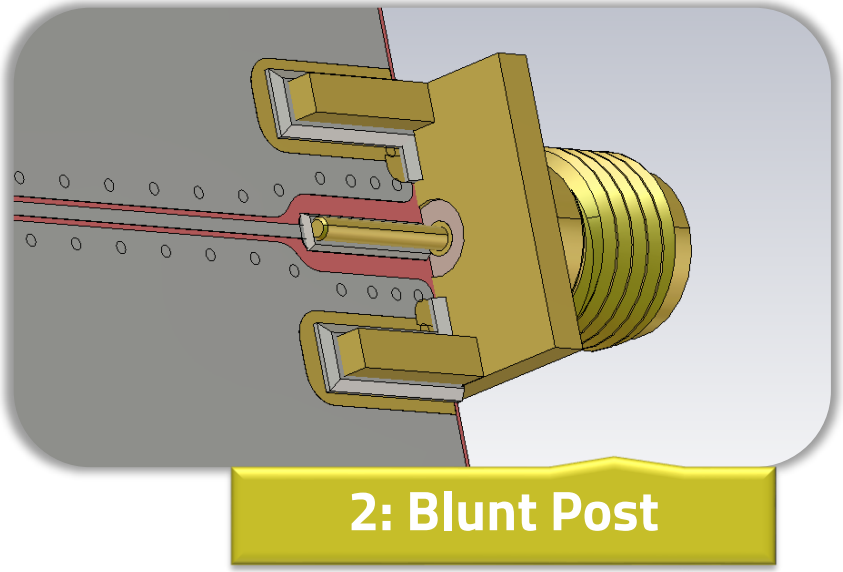
COMBINATION CONNECTOR & PCB: EXAMPLES

CPWG - ROUND VS FLAT: OVERVIEW

- **Analysis of 2 different designs**



1: Flat Tab



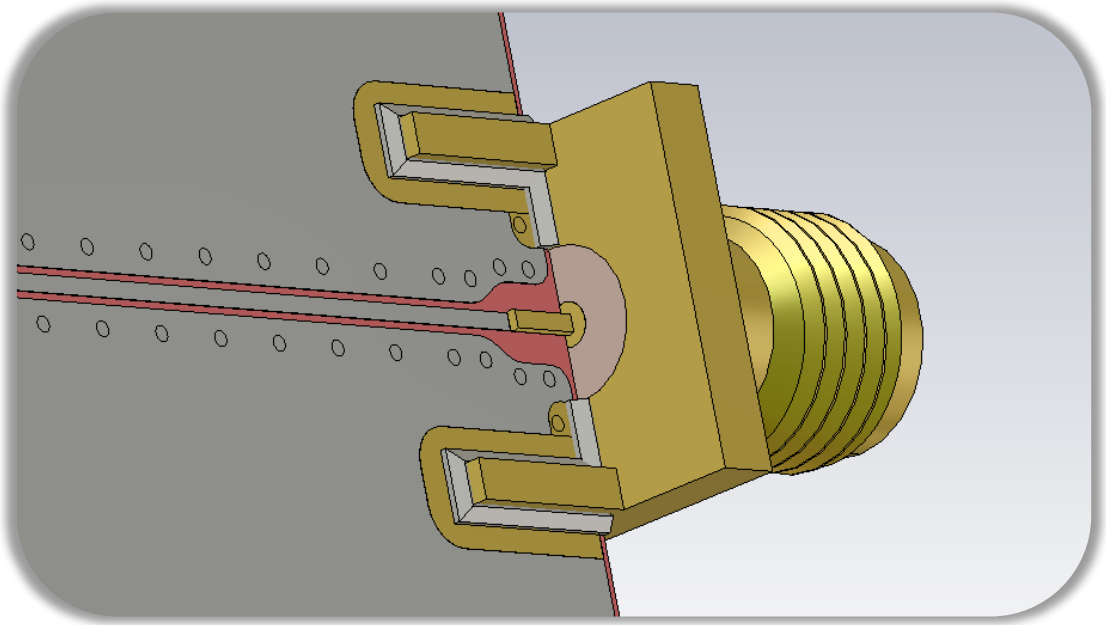
2: Blunt Post

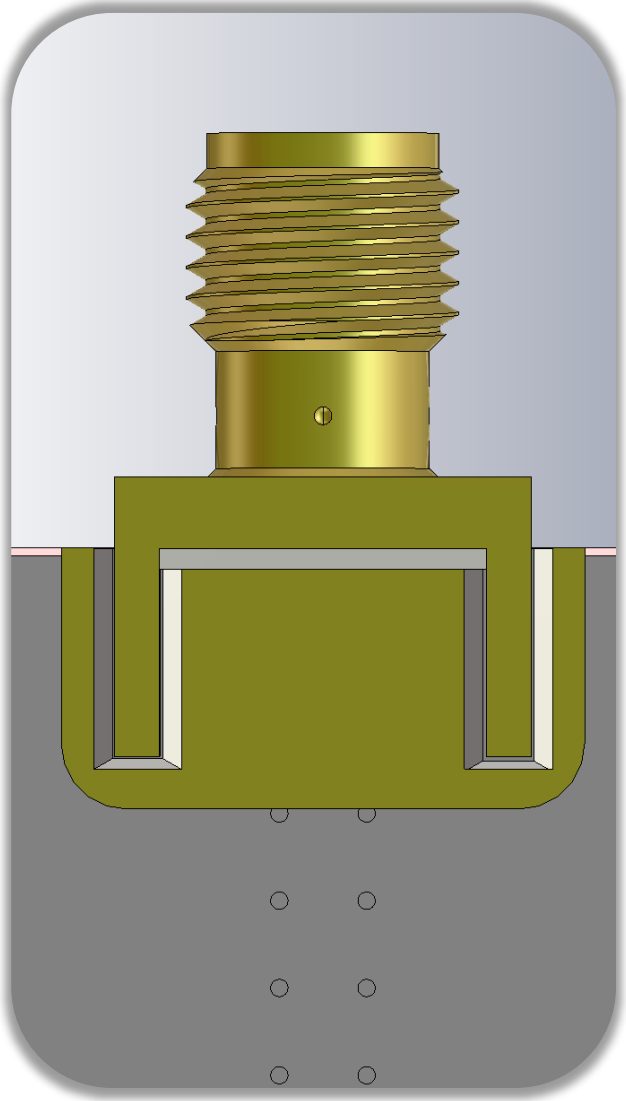
- **Fits to small traces**
  - Easy design
  - Difficult to solder
- **Needs extra solder pad**
  - Difficult design
  - Easy to solder

COMBINATION CONNECTOR & PCB: EXAMPLES

CPWG - FLAT: DESIGN

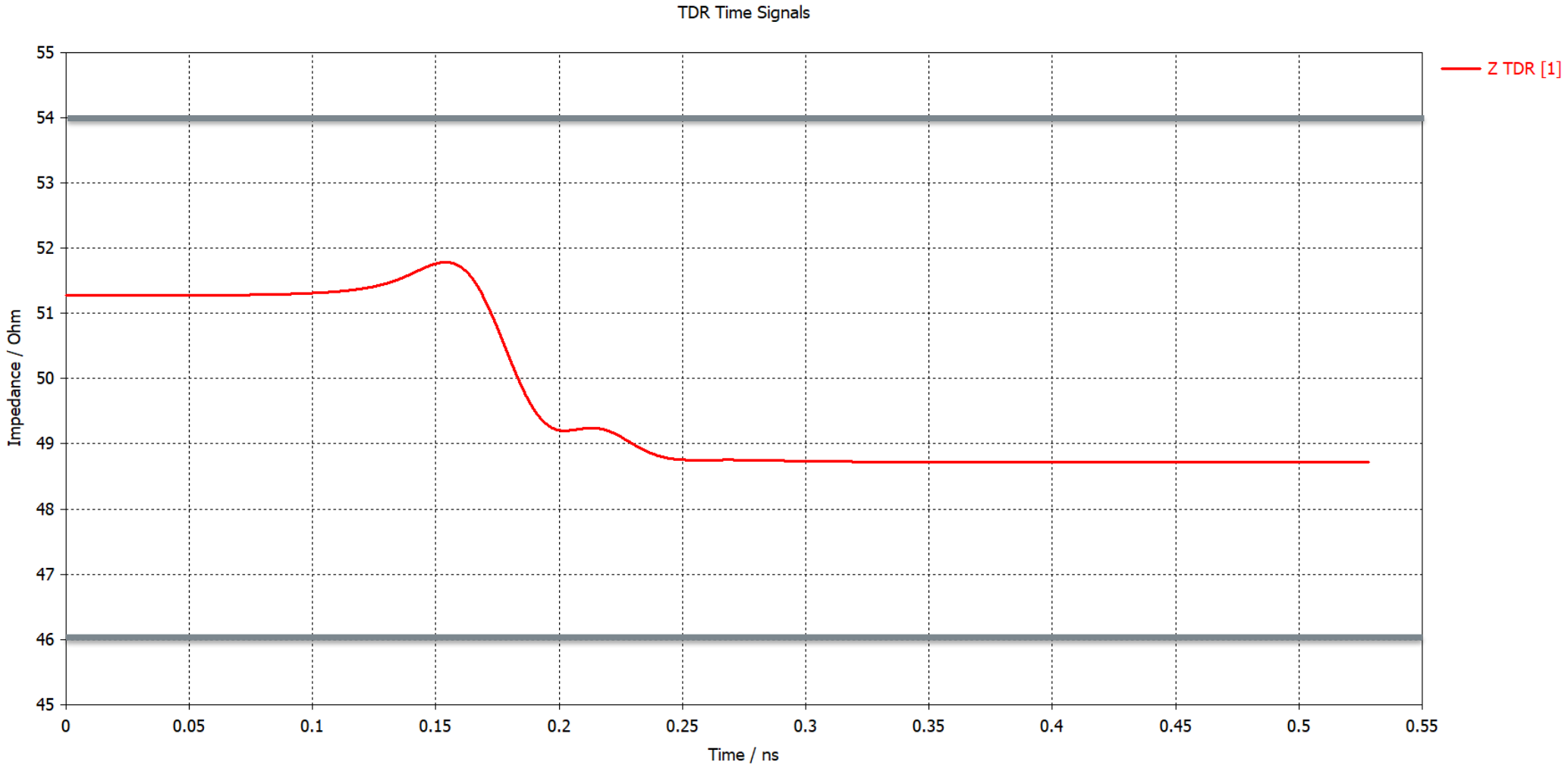
- **Solder pads & several vias**
- **Very good GND connection**
- **Optimized RF-Line with taper**





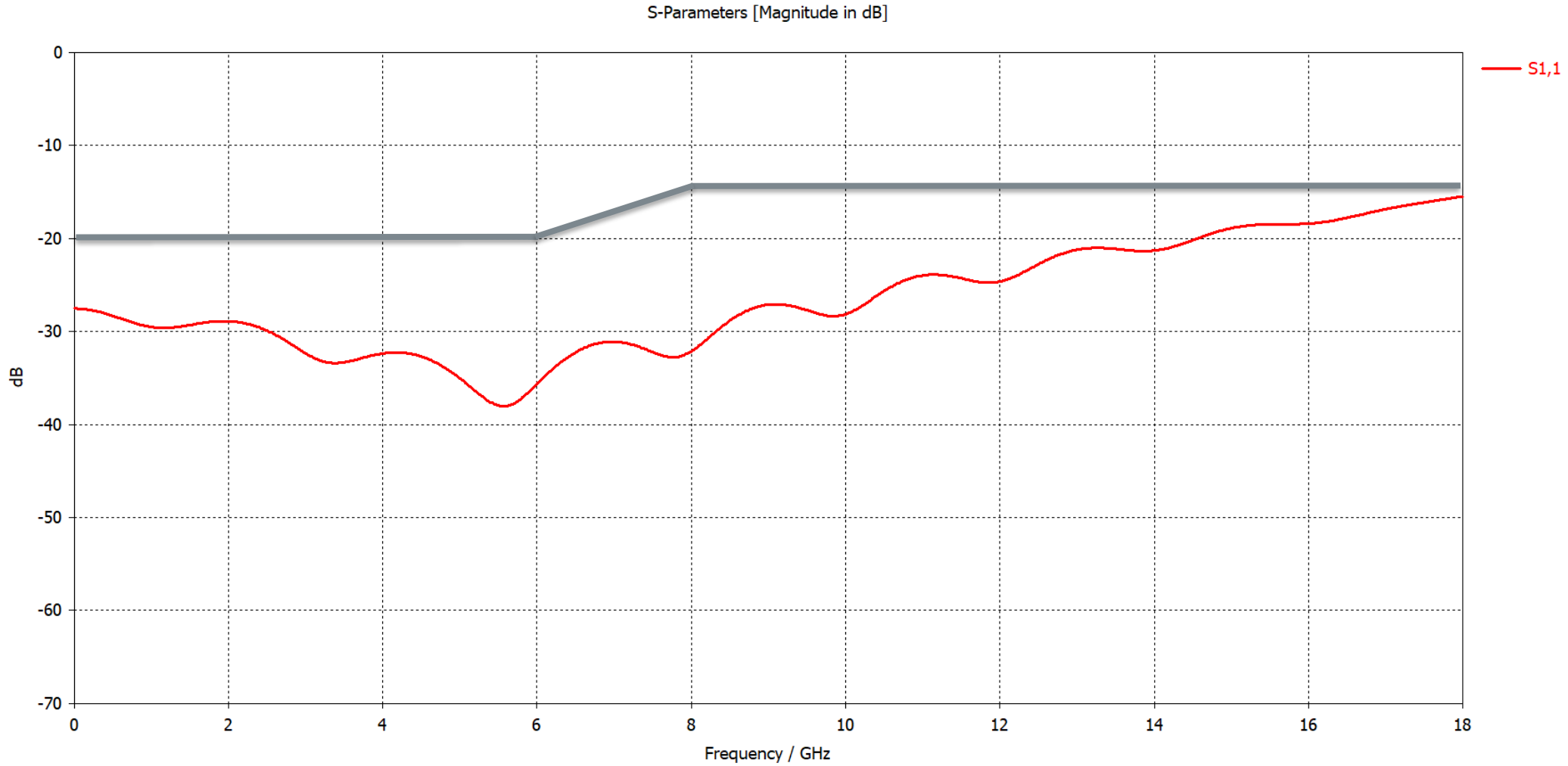
COMBINATION CONNECTOR & PCB: EXAMPLES

CPWG - FLAT: TDR



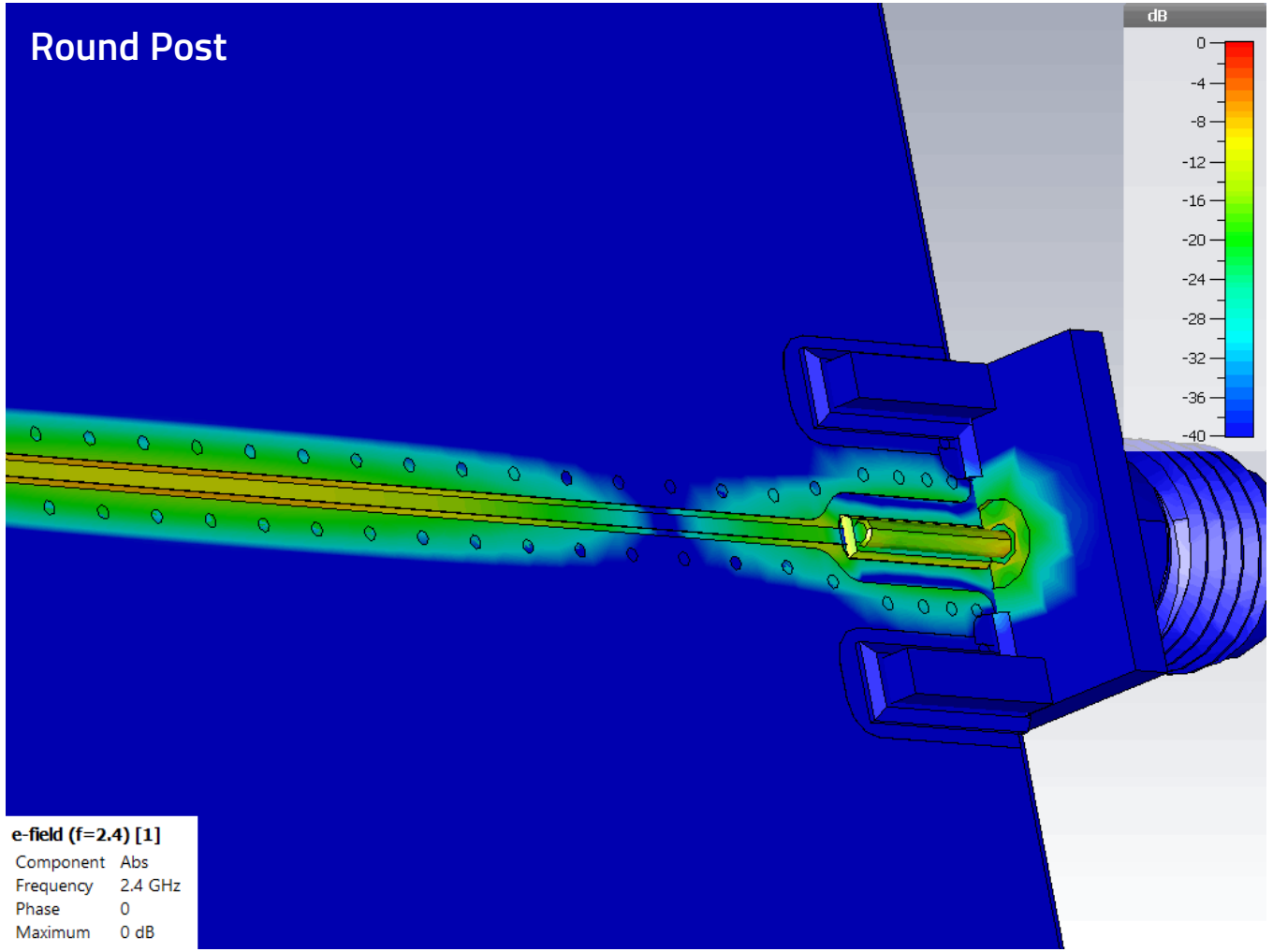
COMBINATION CONNECTOR & PCB: EXAMPLES

CPWG - FLAT: S-PARAMETER



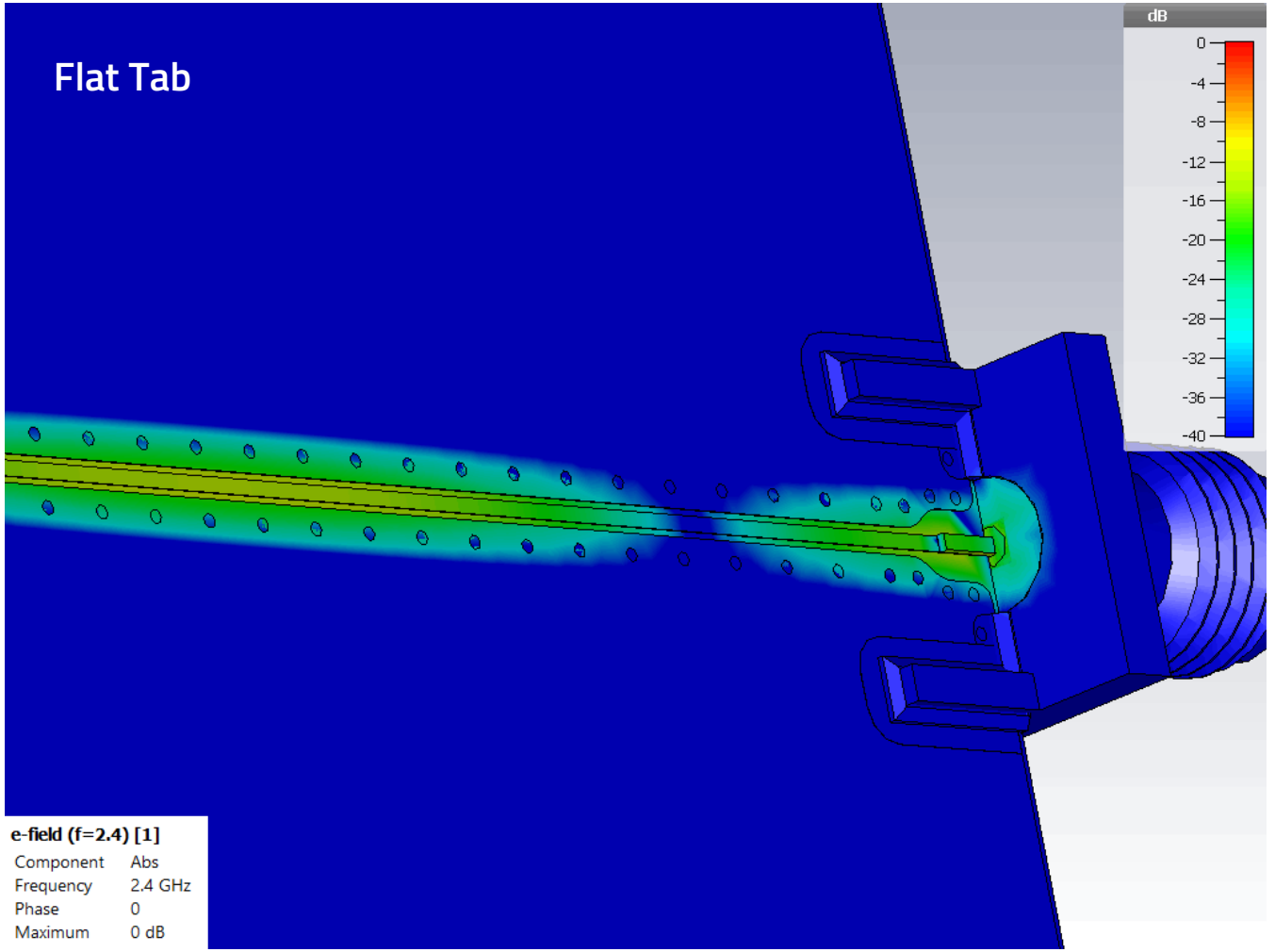
COMBINATION CONNECTOR & PCB: EXAMPLES

CPWG - ROUND: SIMULATION



COMBINATION CONNECTOR & PCB: EXAMPLES

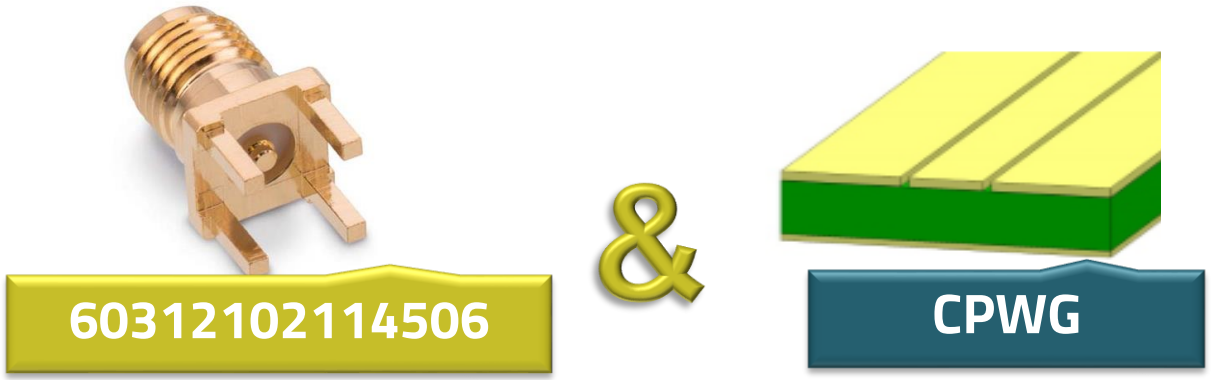
CPWG - FLAT: SIMULATION



COMBINATION CONNECTOR & PCB: EXAMPLES

CPWG - THT: OVERVIEW

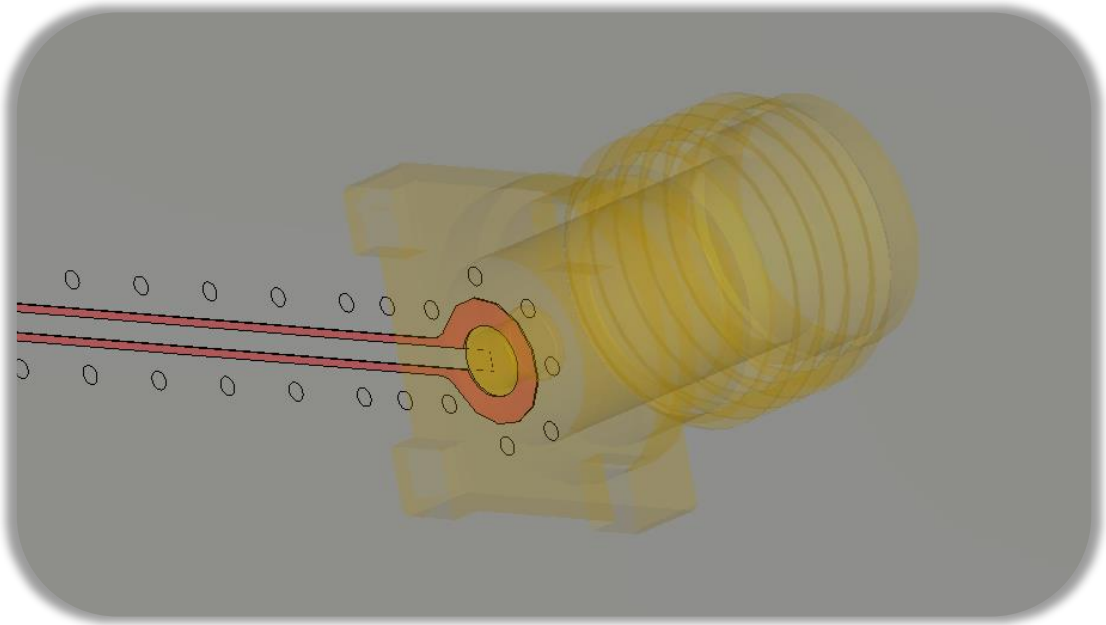
- **Given Task:**
  - THT **60312102114506**
  - 1.55 mm PCB
  - 4 Layers – FR4 Core & Prepreg
  - CPWG
- **Application: Circuit design**

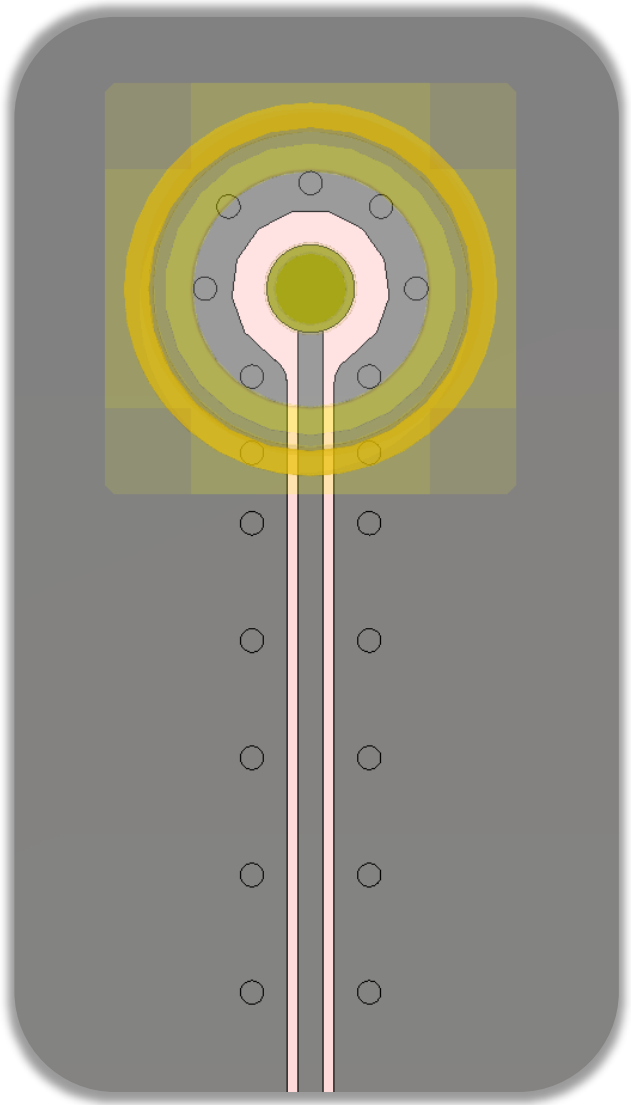


COMBINATION CONNECTOR & PCB: EXAMPLES

CPWG - THT: DESIGN

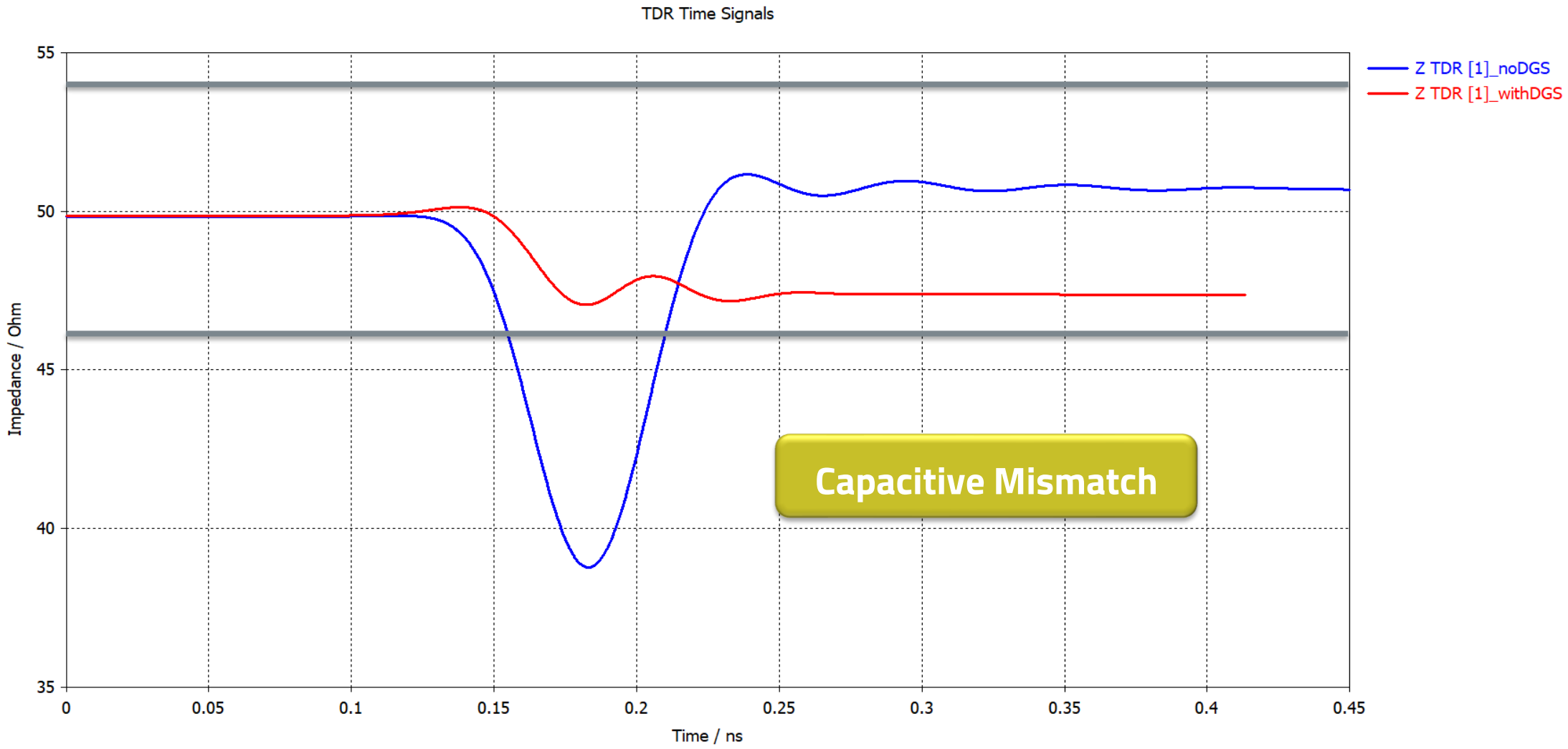
- **Solderpad & several vias**
- **Very good GND connection**





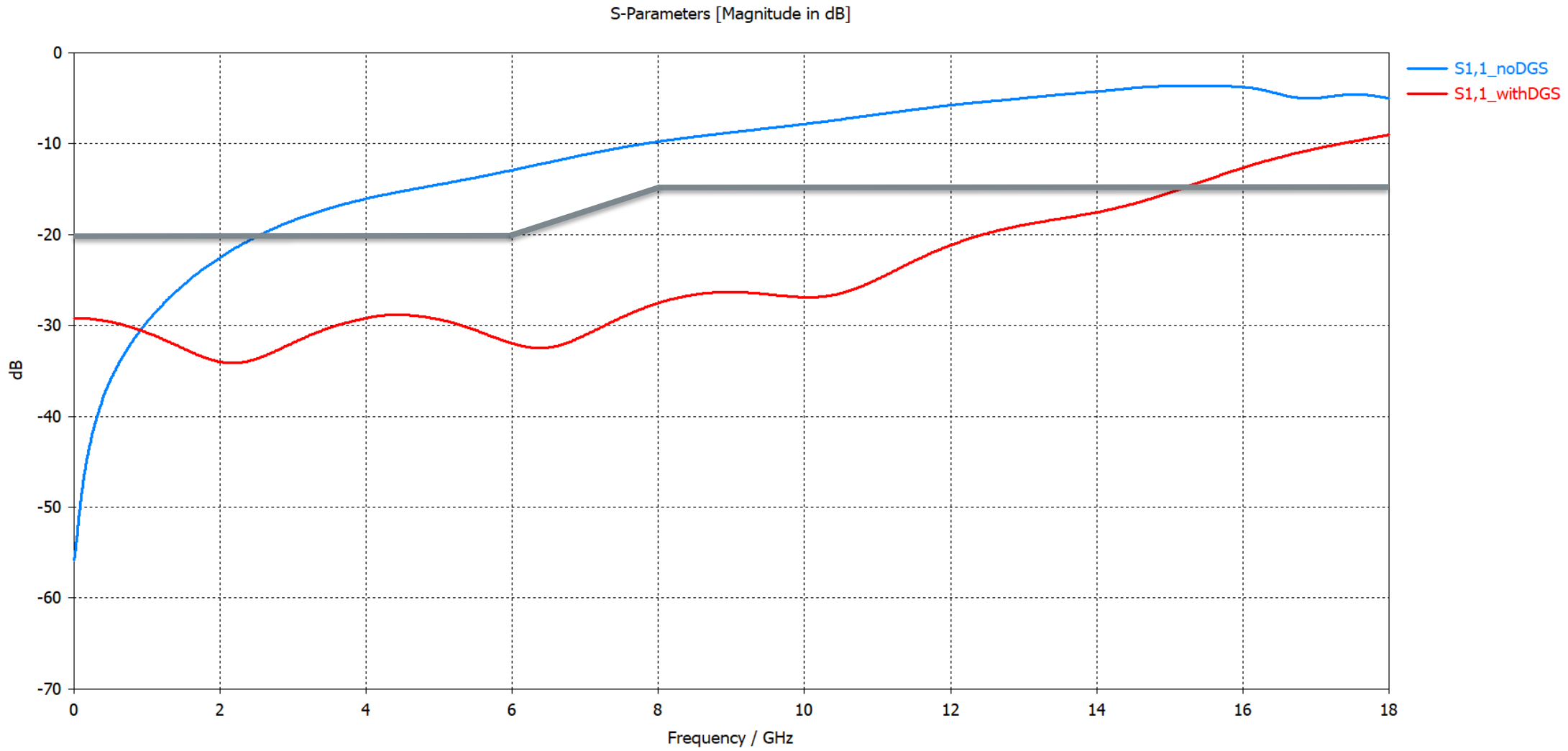
COMBINATION CONNECTOR & PCB: EXAMPLES

CPWG - THT: TDR



COMBINATION CONNECTOR & PCB: EXAMPLES

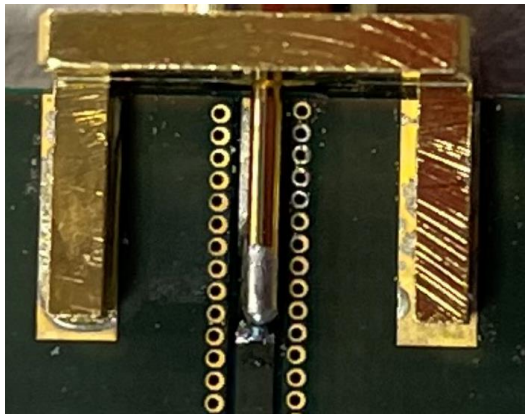
CPWG - THT: S-PARAMETER



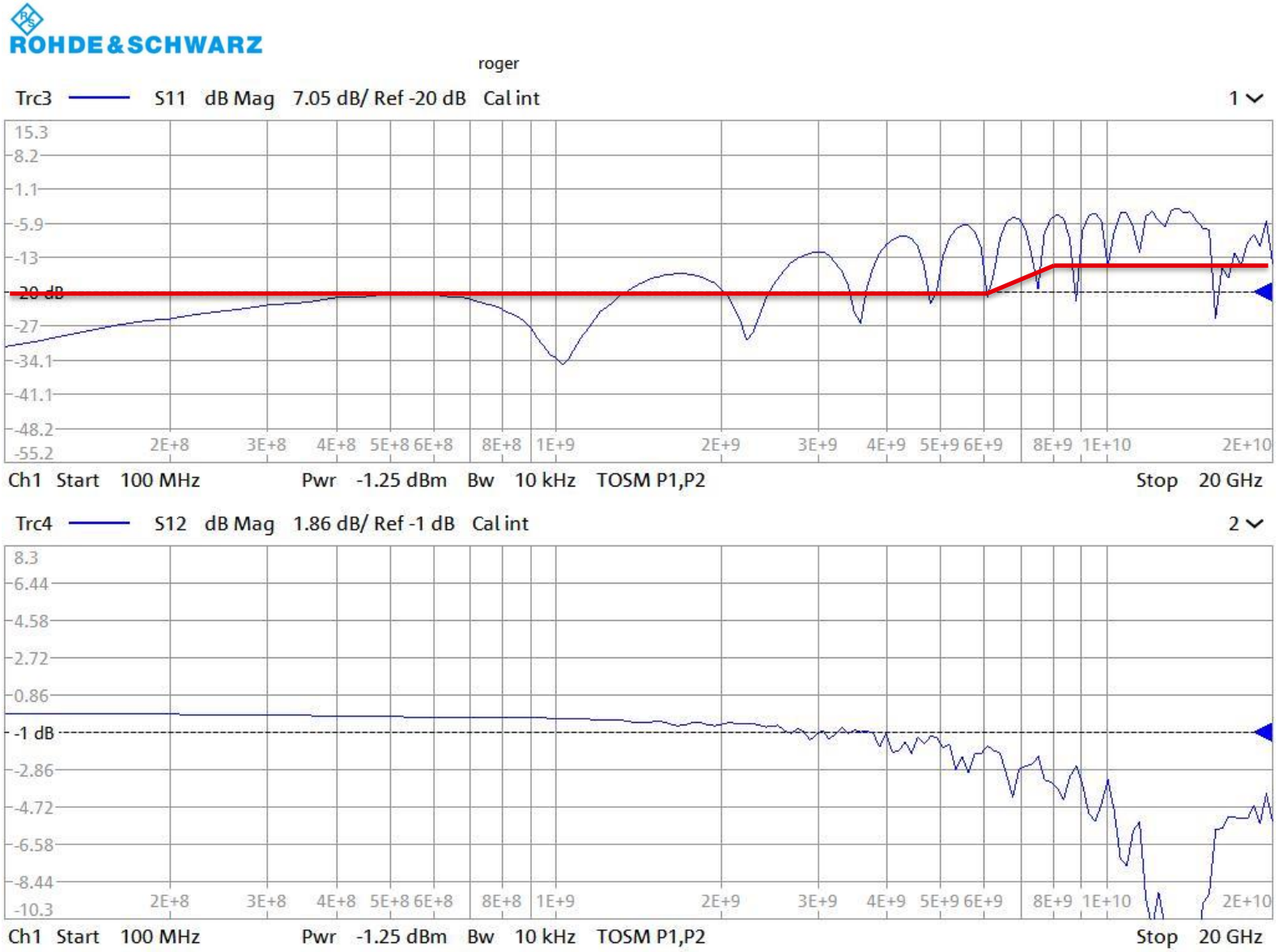
REAL MEASURMENTS

INITIAL WITHOUT TIN

Straight trace
No impedance adjustment



No tin



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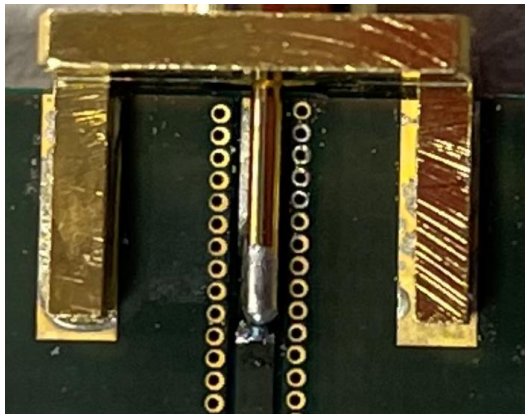
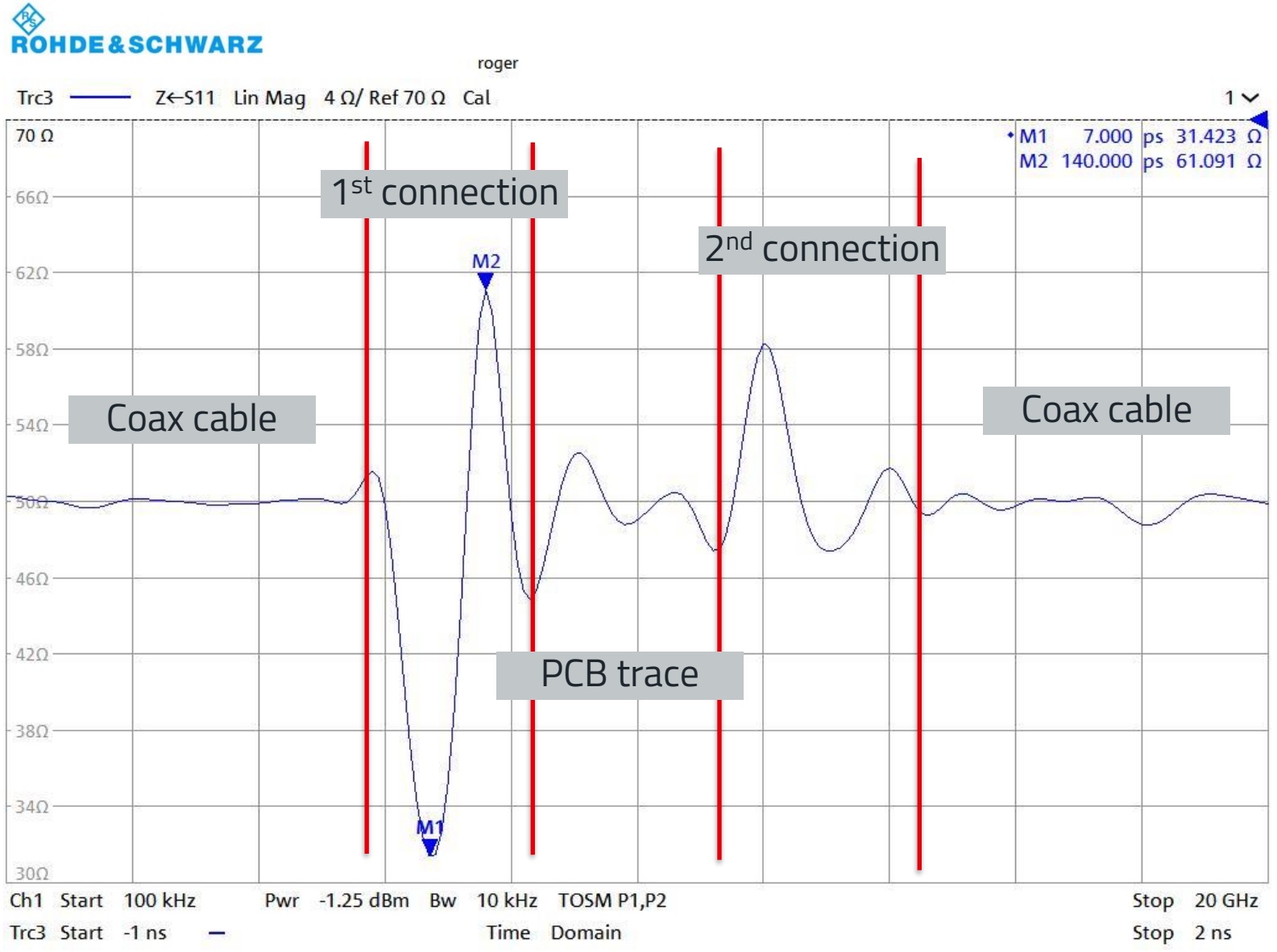


No tin



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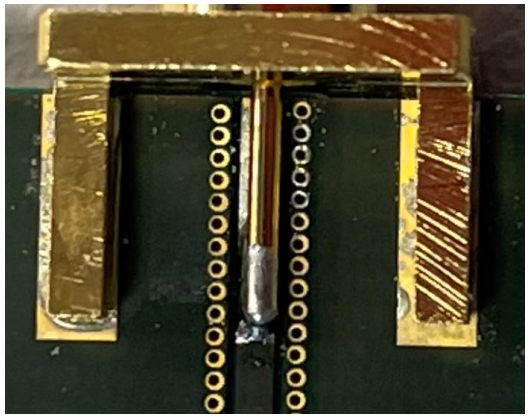
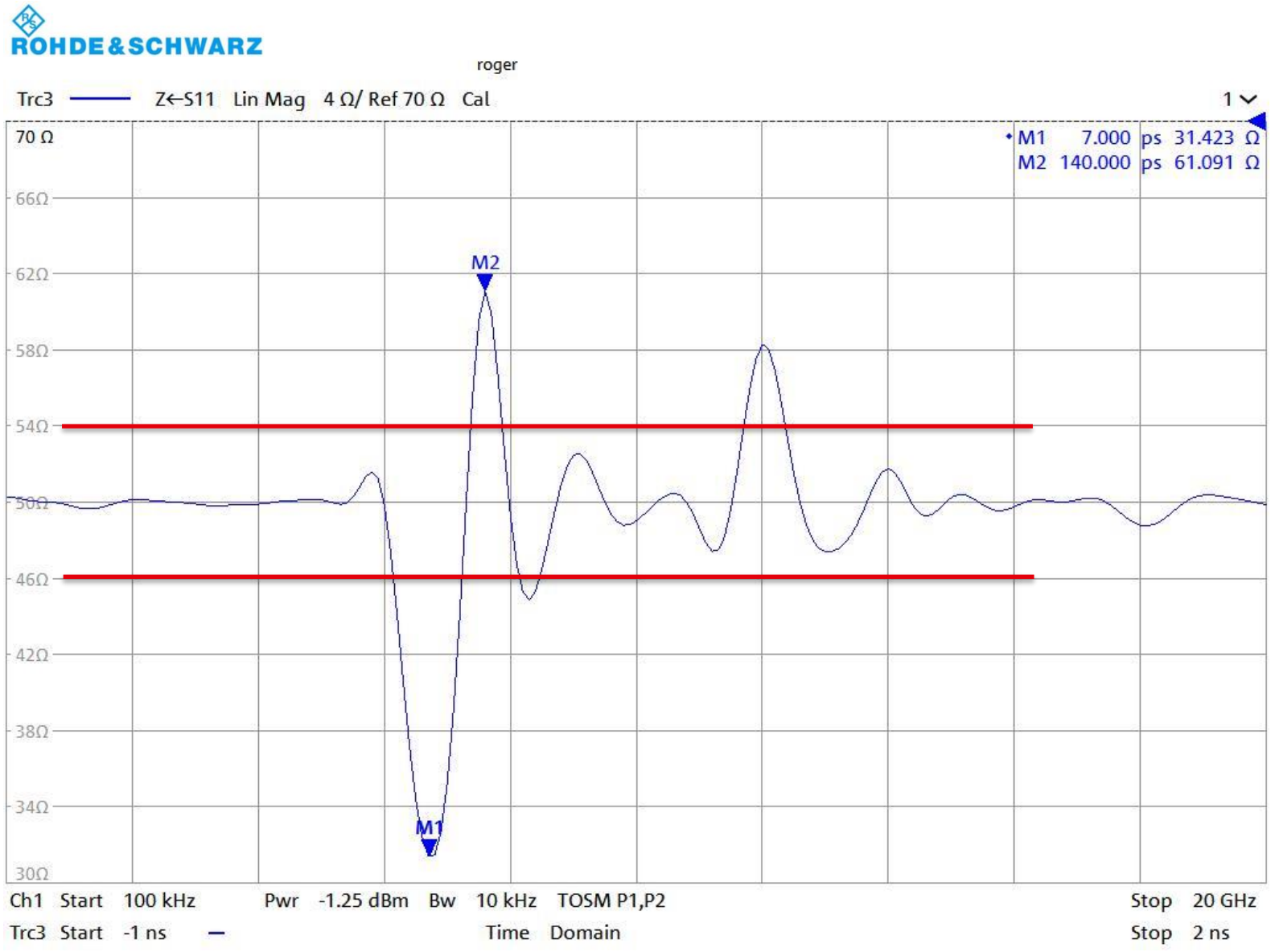


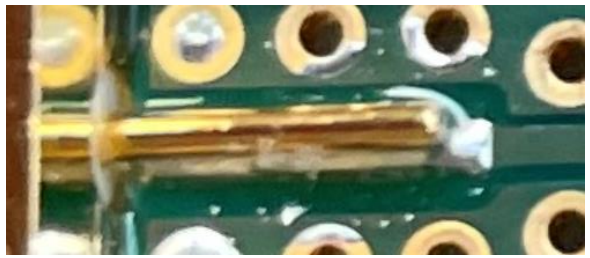
No tin



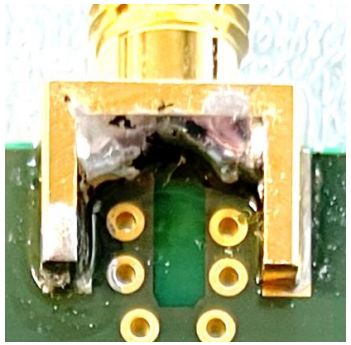
REAL MEASURMENTS

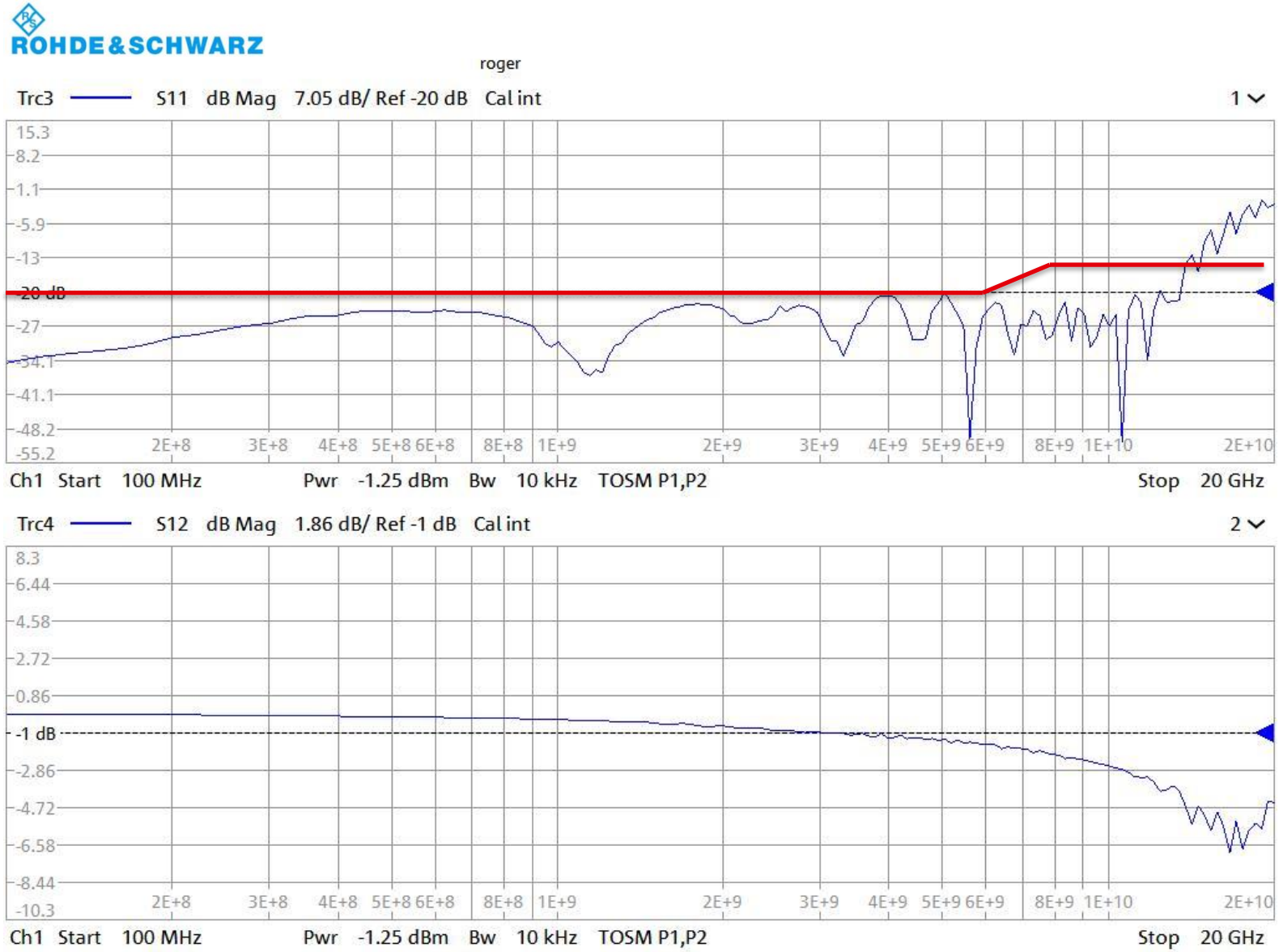
ADJUSTED *SHAPE WITH DGS WITH TIN*

Ground layer adjustment
Adjusted shape



Tin + DGS





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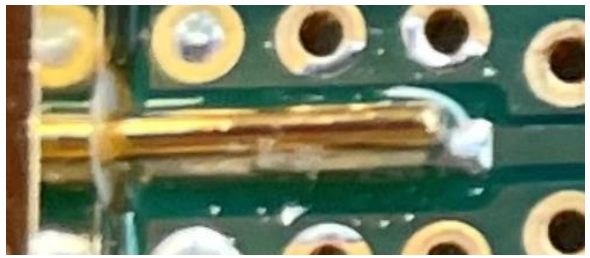
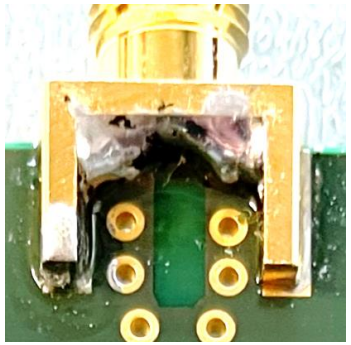


Tin + DGS



CONCLUSIONS

Impedance adjustment is important above 500MHz and necessary above 1GHz

It is easy to improve signal integrity:

Use capacitance adaptation, DGS	Avoid soldermask on RF-lines	Use GND via stitching (holes ~ 0,3mm enough)

DZIĘKUJĘ ZA UWAGĘ

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