Od pomysłu do zwycięstwa – nasz sukces w International Future Energy Challenge 2025

Hardware Design Masterclasses, 28.11.2025
Paweł Wodzyński

Faculty of Electrical Engineering
Warsaw University of Technology

Agenda

1. Czym jest IFEC?
2. Tematyka konkursu
3. Nasz zespół – jak to się zaczęło
4. W stronę zwycięstwa na Tajwanie
5. Nasze rozwiązanie
6. Proces projektowania
7. Finalne wyniki
8. Q&A

International Future Energy Challenge

- Największy międzynarodowy konkurs studencki
- Ponad 20 lat tradycji
- Współpraca z przemysłem
- Wspierany przez największe organizacje

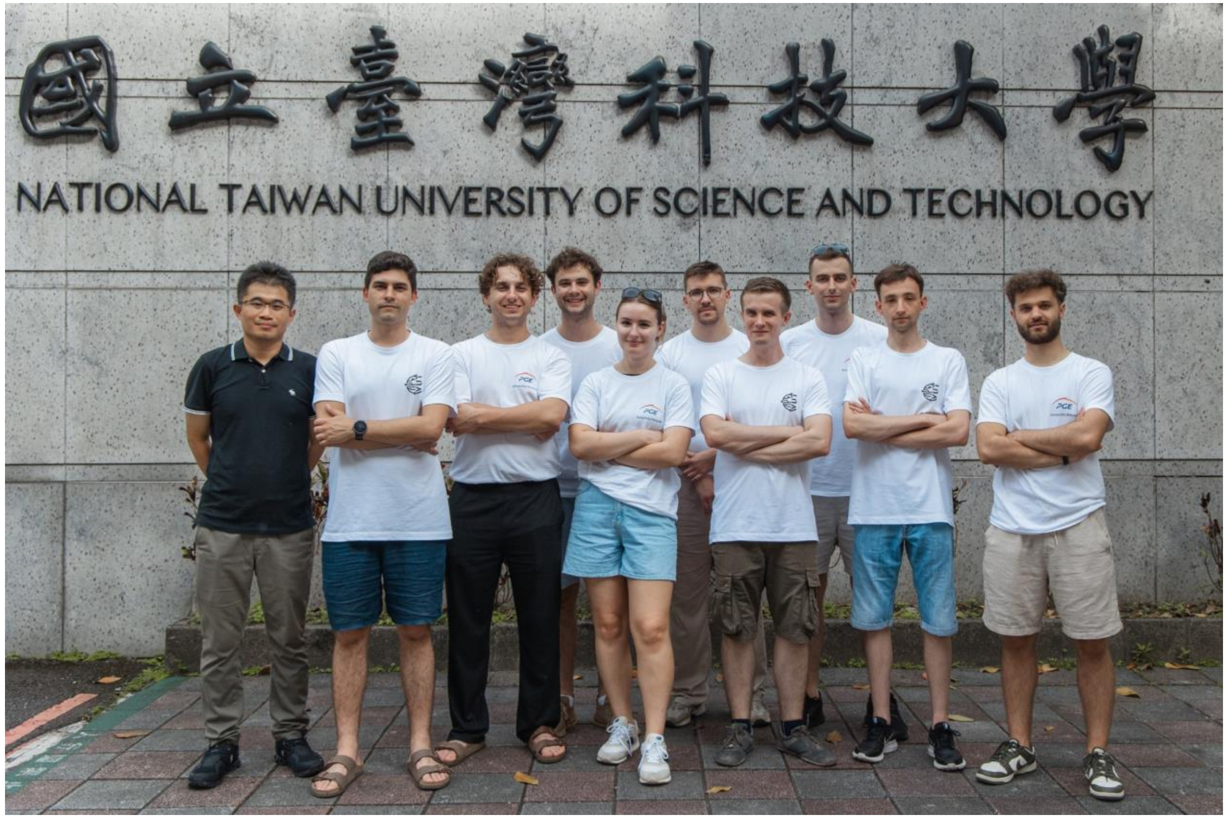
Tematyka poprzednich edycji International Future Energy Challenge

- 2021 Power Supply for Nano Satelites
- 2022 Smart, Efficient and Light Solar Microgrid Inverter
- 2023 Single-Phase Solid State Transformer
- 2024 Audio amplifier
- **2025 Isolated DC-DC Converter with Fast Transient Response and Low Noise**
- 2026 Affordable Bidirectional Onboard Charger for Electric Vehicles

Zespół IFEC

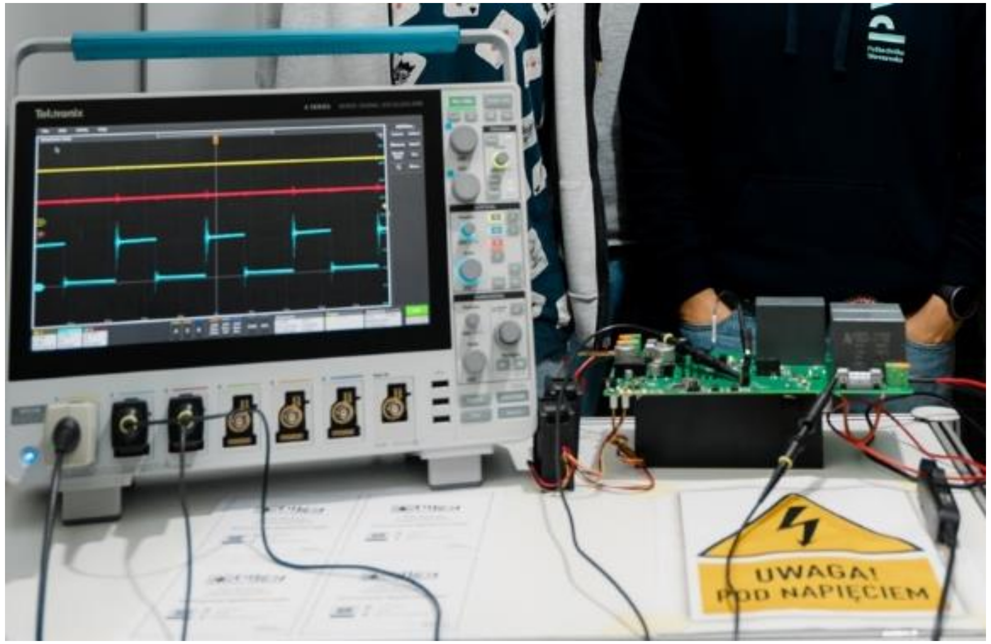
Koło Naukowe
Drones Renewables

Koło Naukowe
Power Electronics And Plasma Applications



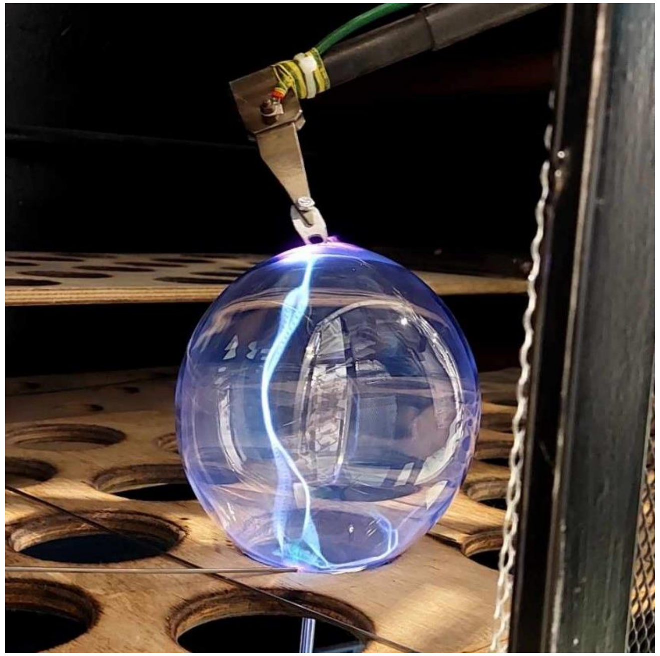
Zespół IFEC

Koło Naukowe
Drones Renewables



Mobilna stacja ładowania dronów

Koło Naukowe
Power Electronics And Plasma Applications



Wzbudzenie plazmy za pomocą wysokoczęstotliwościowego przekształtnika

Zespół IFEC

Mgr inż. Krzysztof
Kalinowski

Od lewej:
Tomasz Zakrzewski
Przemysław Kinasz
Jakub Pykacz
Adrian Ośka
Michał Ptak
Krzysztof Kalinowski
Adrianna Machulak
Paweł Wodzyński
Natalia Wnęk
Błażej Skrzypkowski

Prof. dr hab. inż. Jacek
Rąbkowski

Etapy konkursu IFEC 2025

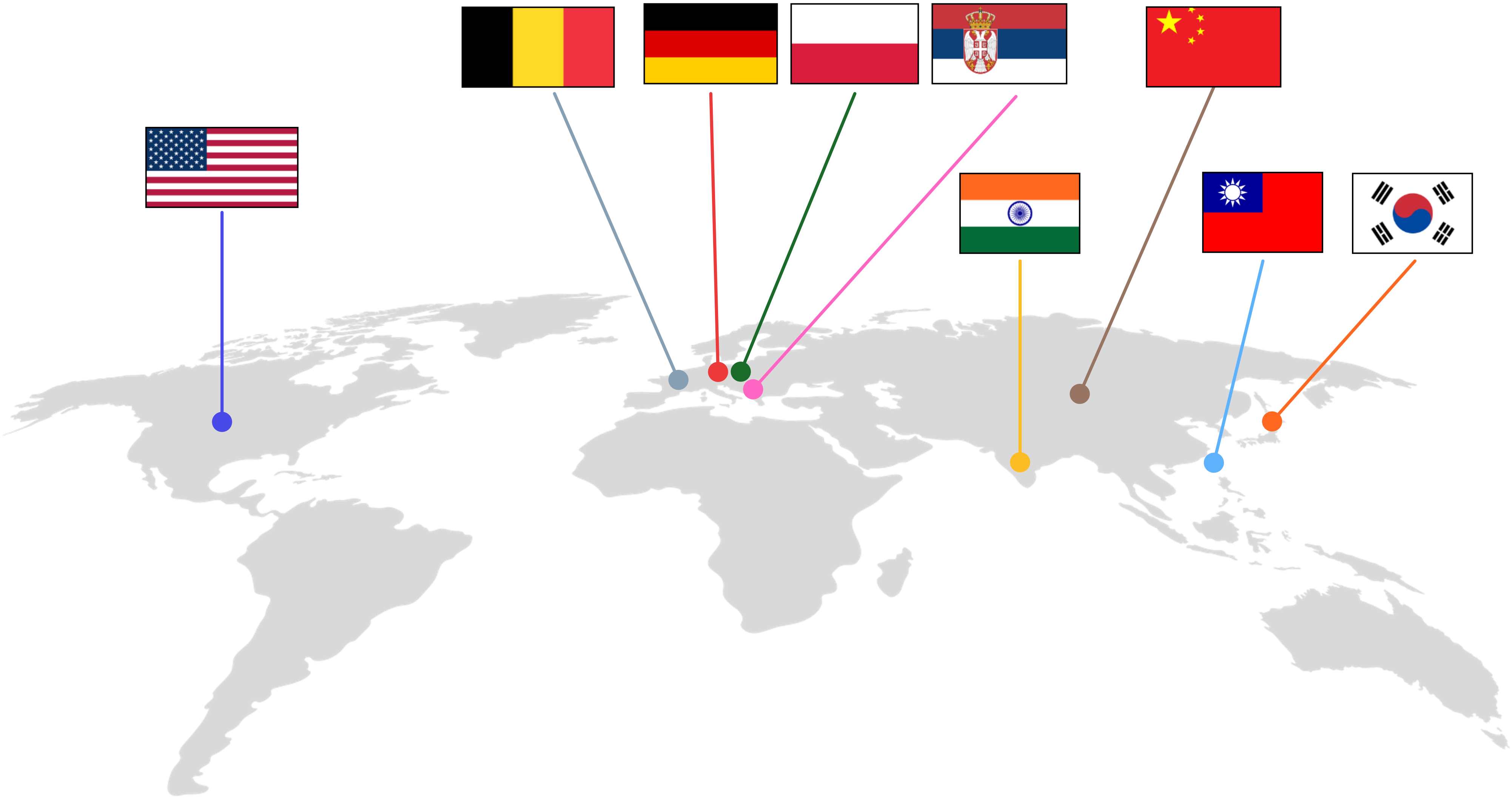
1.10.2024
ogłoszenie wymagań
projektowych

29.11.2024
wysłanie proposala
z koncepcją rozwiązania

16.03.2025
Półfinał
Atlanta, USA

15-19.07.2025
Finał
Tajpej, Tajwan

Półfinał konkursu w Atlancie, USA – 13 zespołów z 9 krajów



Półfinał konkursu w Atlancie, USA – konferencja APEC

Zespoły IFEC 2025

University	Country
Bharatiya Vidya Bhavan's Sardar Patel Institute of Technology	India
KU Leuven and UHasselt (Hasselt University)	Belgium
Huazhong University of Science and Technology	China
Konkuk University	South Korea
National Formosa University	Taiwan
National Kaohsiung University of Science and Technology	Taiwan
Reutlingen University	Germany
The University of Connecticut	United States
University of Belgrade	Serbia
University of Rhode Island	United States
University of Texas at Austin	United States
Utah State University	United States
Warsaw University of Technology	Poland

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Finał na Tajwanie – Chroma ATE

Grand Prize
Warsaw University of Technology,
Poland

Wytyczne - Isolated DC-DC Converter with Fast Transient Response and Low Noise

Input Voltage
400Vdc (400–600µF @ ≥450V)

Output Voltage
20–150Vdc (<0.5% accuracy)

Output Current
Max 10Adc

Rated Power
1.5kW@150V, 600W@60V, 200W@20V

Load Response
±200mV within 100µs (0–10A)

Step Response
Rise <100µs, Fall <1ms

Regulation
<0.1% @ 20V, 60V, 150V

Ripple & Noise
<200mVp-p/30mVrms (20MHz BW)

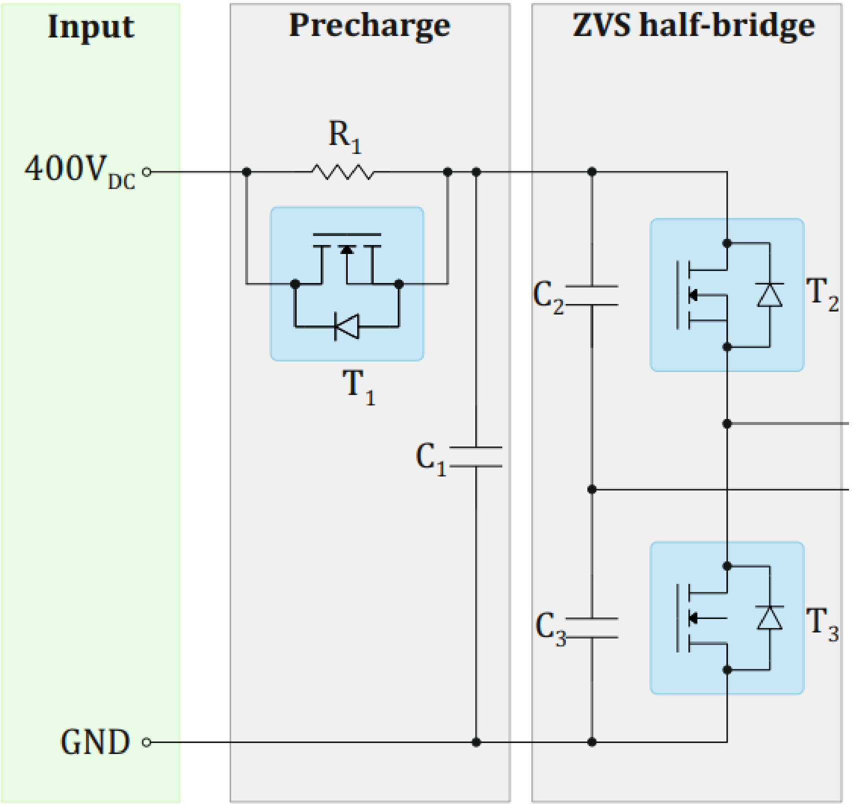
Efficiency
>92%@25%, >96%@50%, >95%@100%

Power Density
>1.6W/cm^3

OCP & OL
12 A for 2s
≥13 A - OFF (< 100ms)

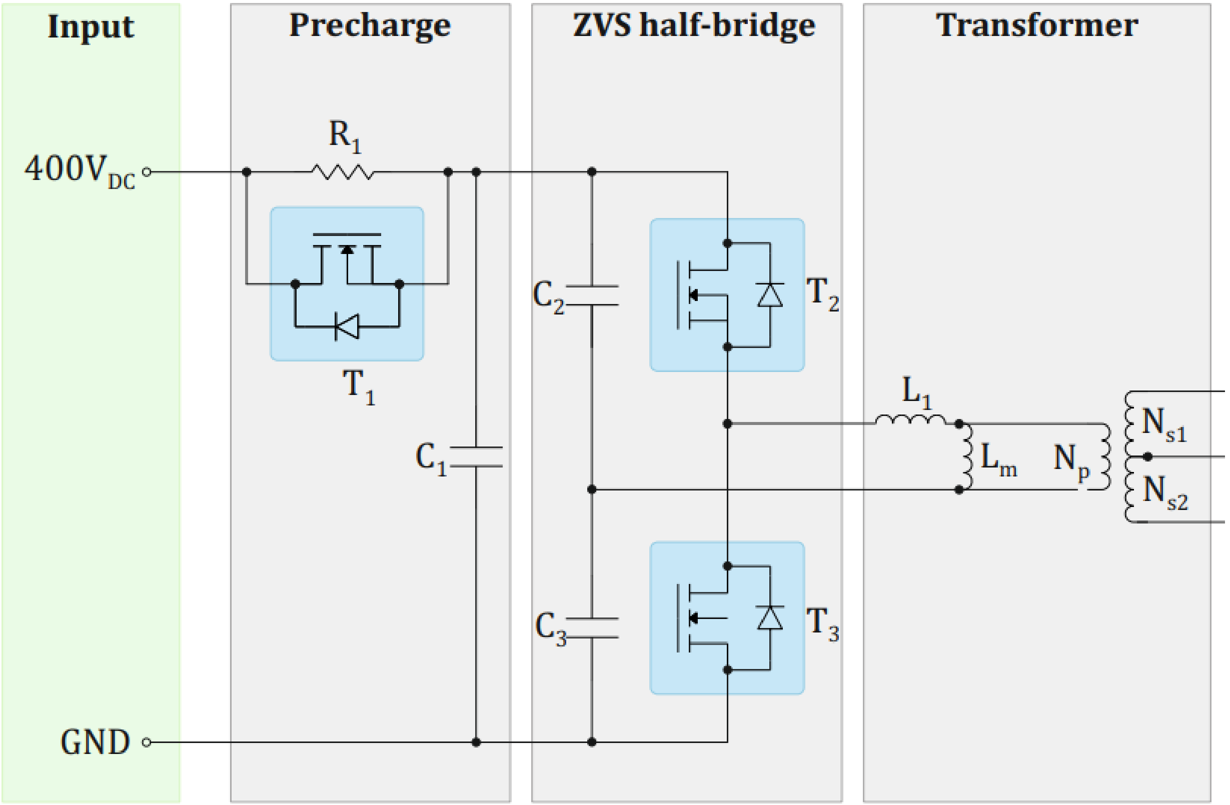
Thermal & Safety
Air cooling only
No burn-in damage
(150V, 10min, 60°C±5)
Galvanic isolation 1.5kVac

Koncepcja techniczna



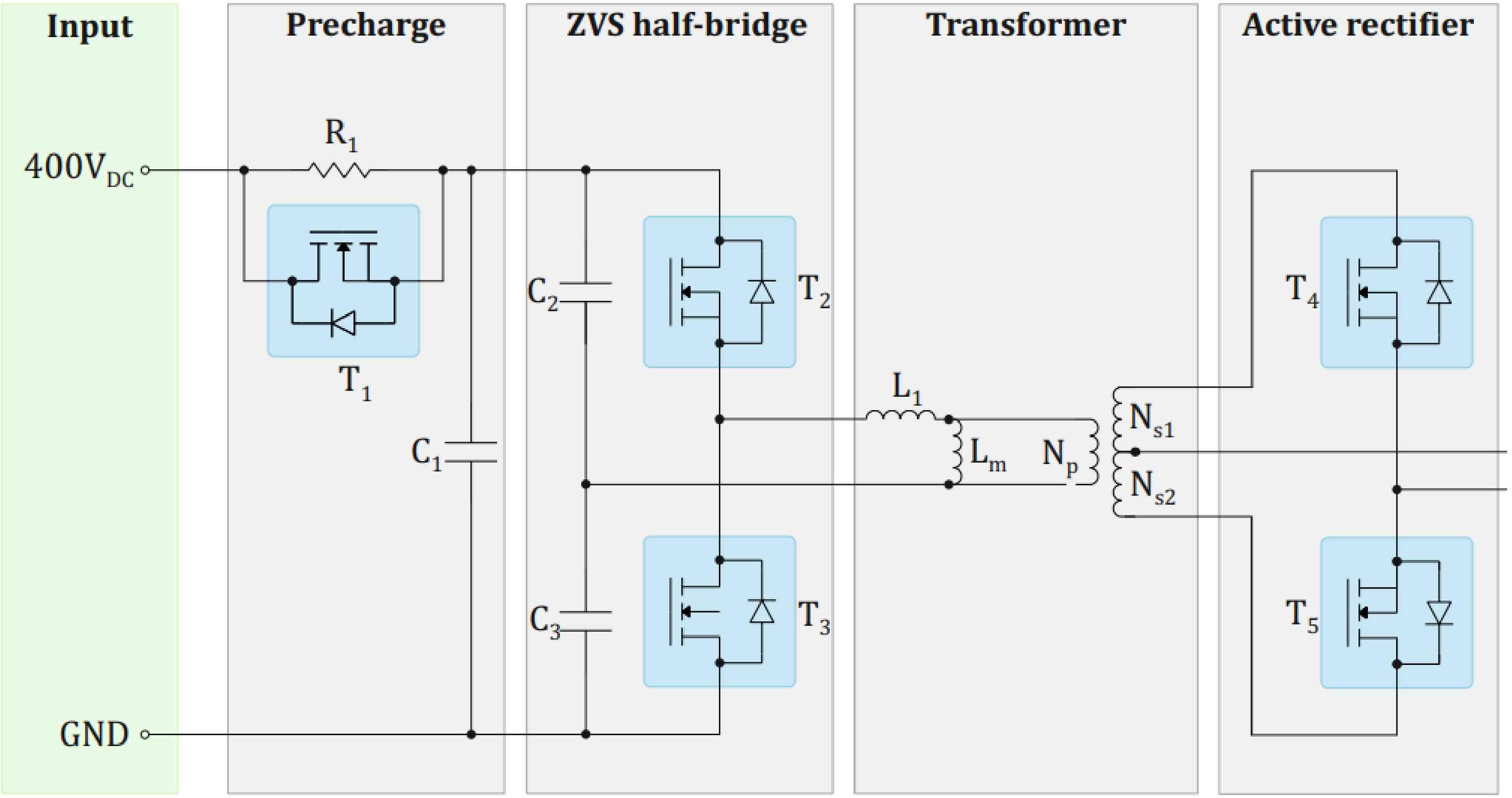
$400V_{DC}$ $200V_{AC}$

Koncepcja techniczna



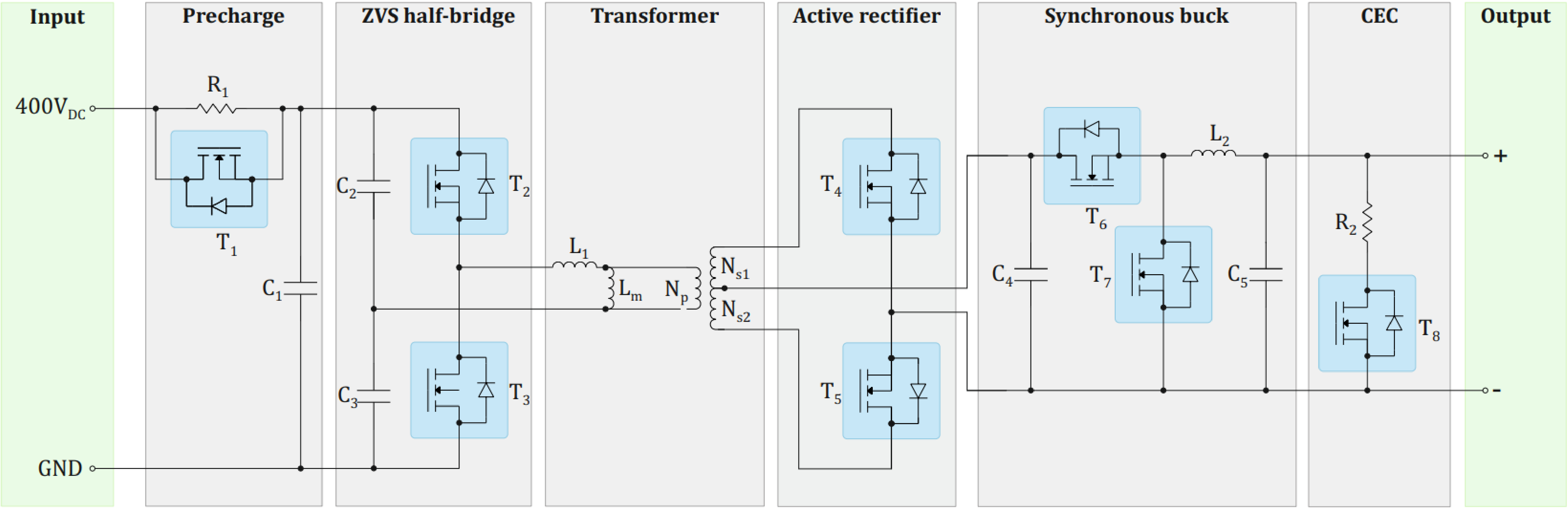
$400V_{DC}$ $200V_{AC}$ 7:6:6

Koncepcja techniczna



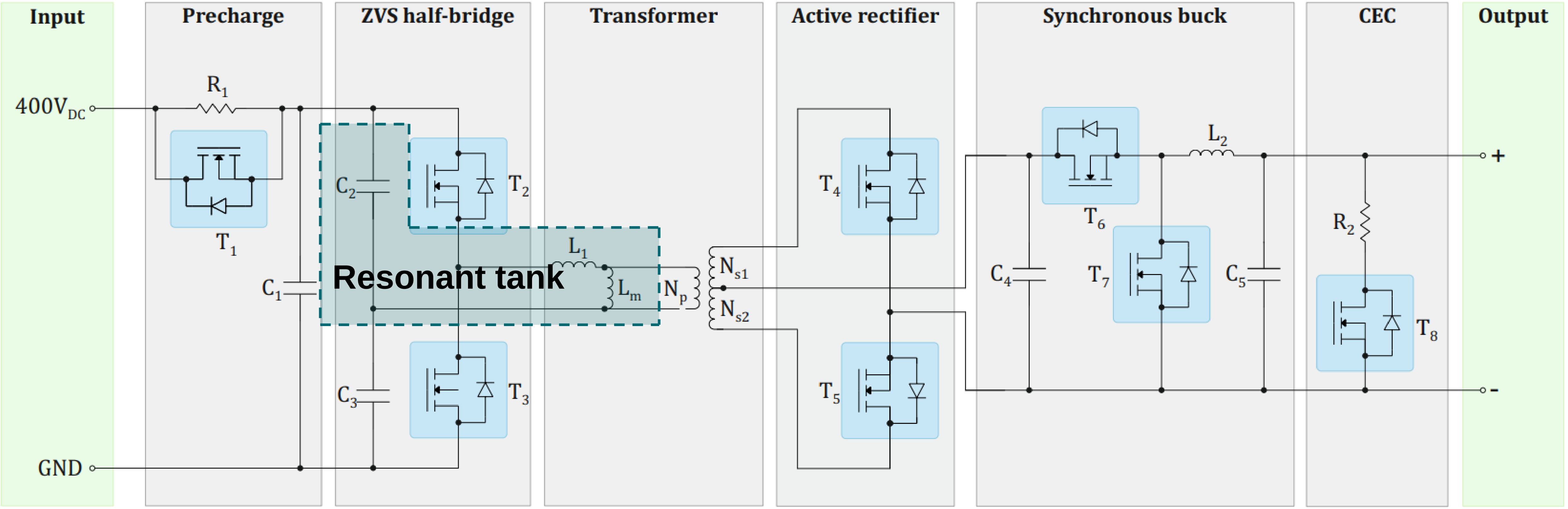
$400V_{DC}$ $200V_{AC}$ 7:6:6 ~$180V_{DC}$

Koncepcja techniczna



$400V_{DC}$ $200V_{AC}$ 7:6:6 $\sim 180V_{DC}$ $20\text{-}150V_{DC}$

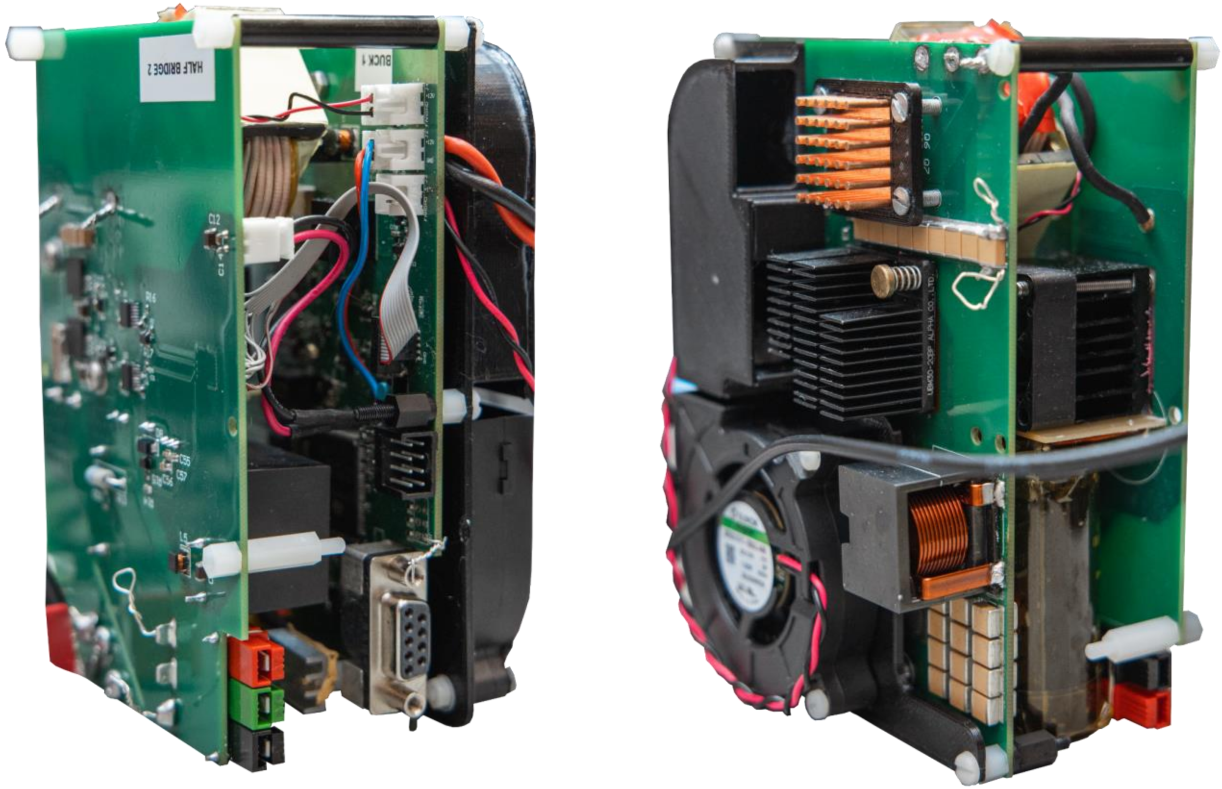
Koncepcja techniczna



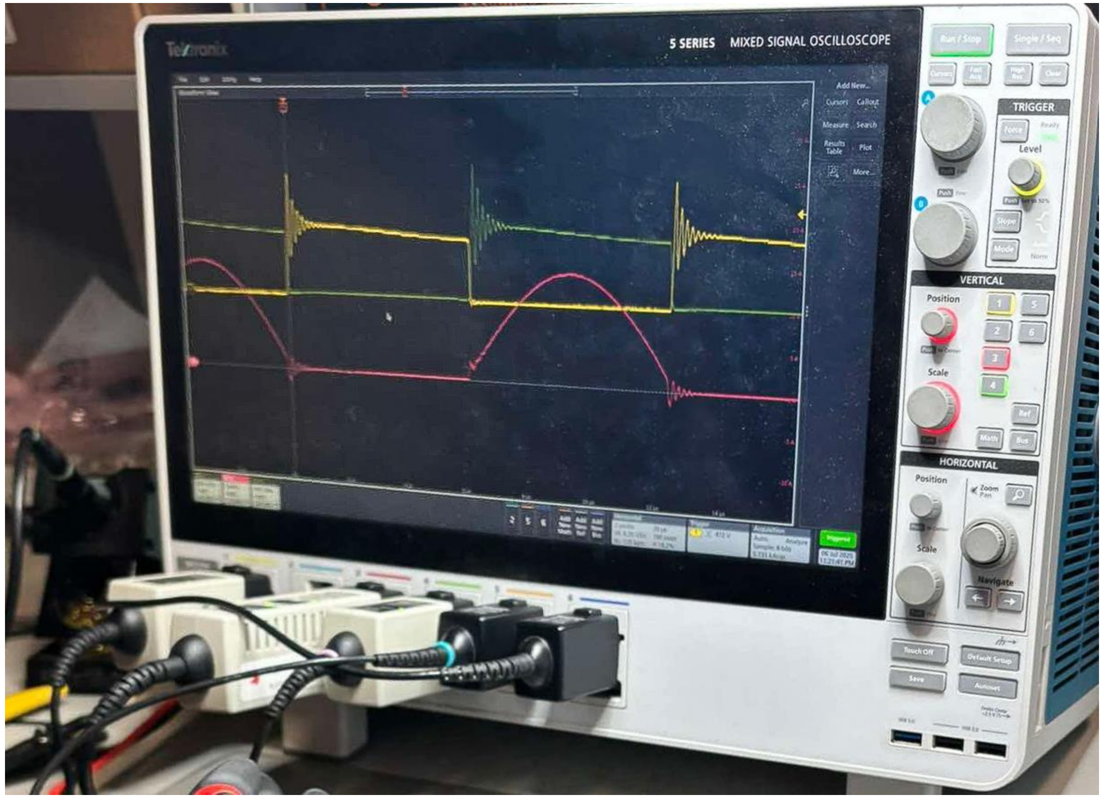
$400V_{DC}$ $200V_{AC}$ 7:6:6 $\sim 180V_{DC}$ $20\text{-}150V_{DC}$

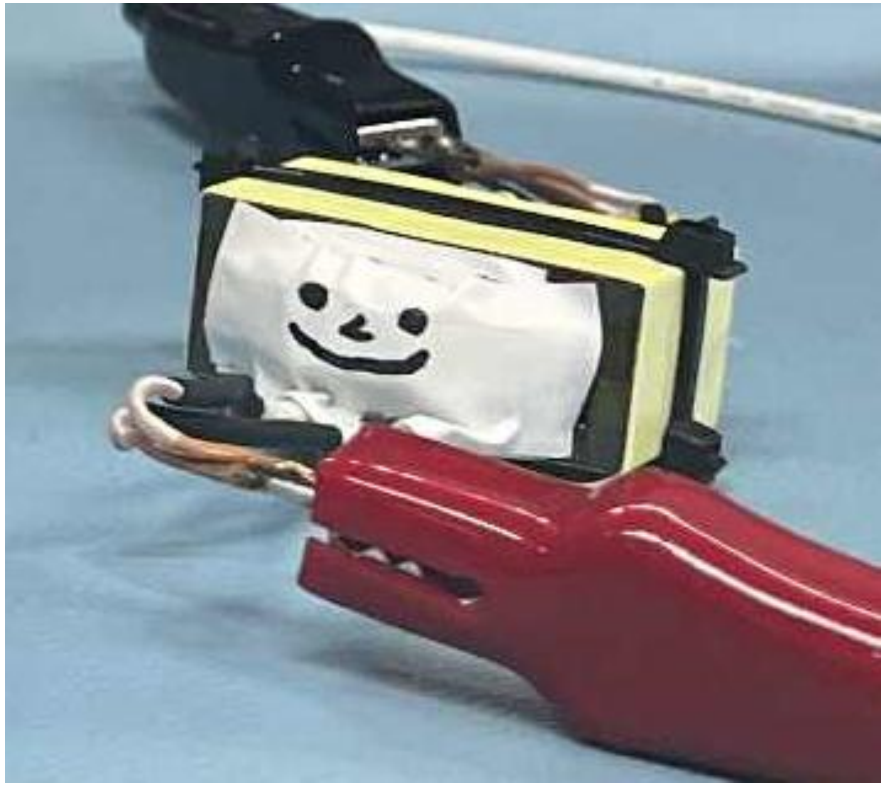
Finalna koncepcja projektowa

- 2 stopnie konwersji
    - 1. stopień – GaN half-bridge with SiC rectifier (80 kHz)
    - 2. stopień– GaN Synchronous Buck (200 kHz)
- sterowanie oparte na STM32H7 (dual core)
- nisko-profilowy transformator
- system dwukanałowego chłodzenia powietrzem
- kompaktowy kształt

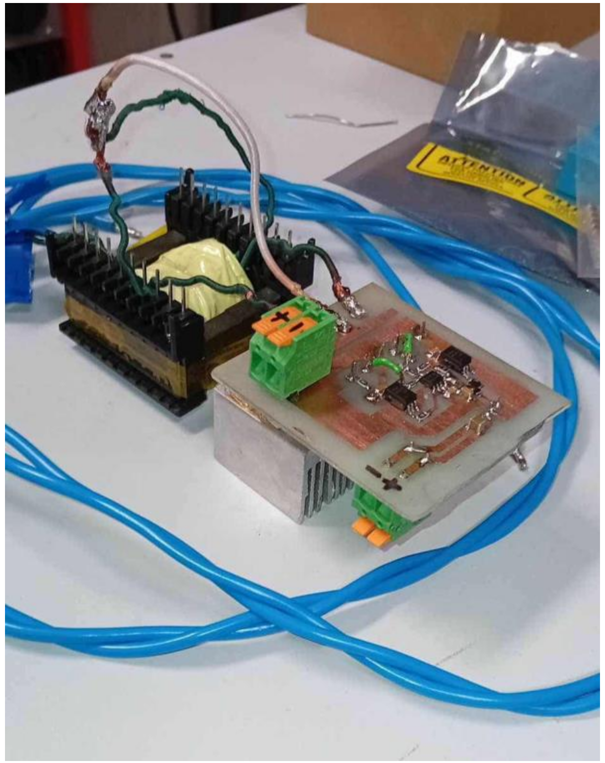


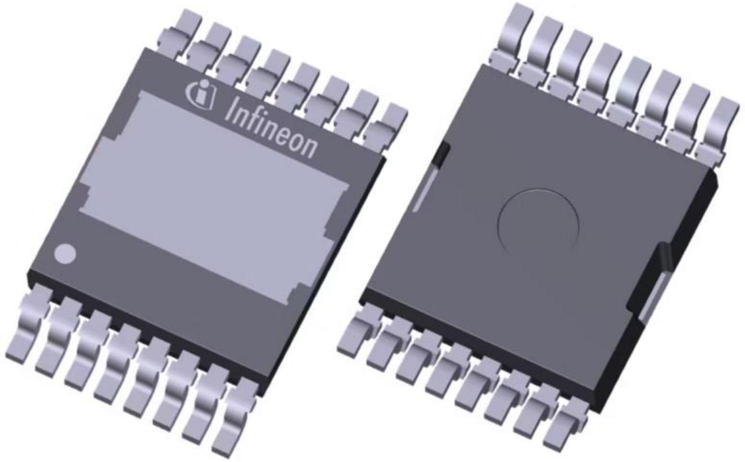
Optymalizacja sprawności





Proces prototypowania prostownika aktywnego





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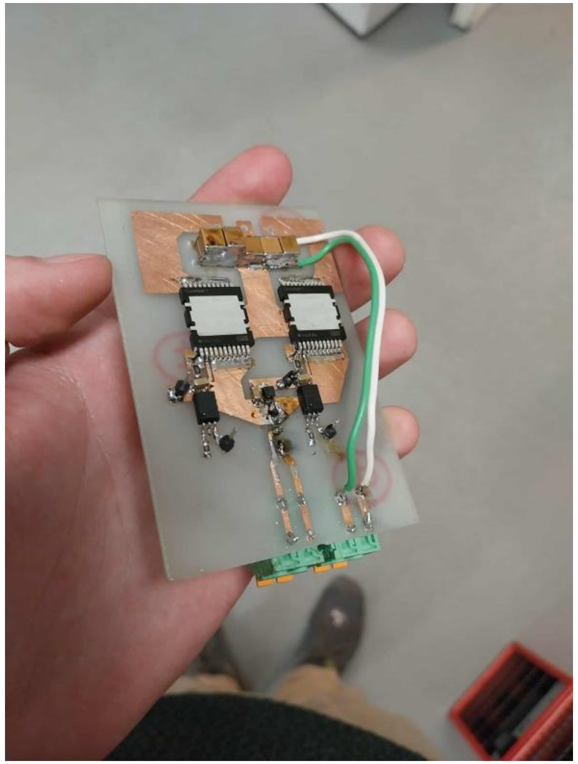
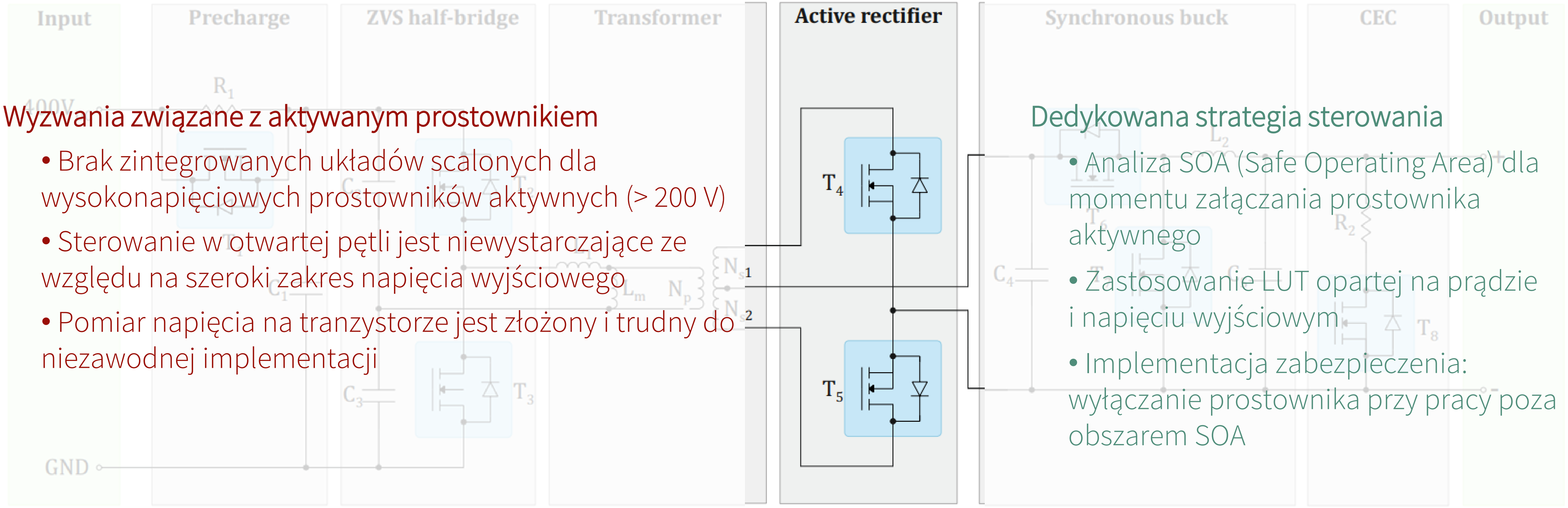


Sterowanie prostownika aktywnego



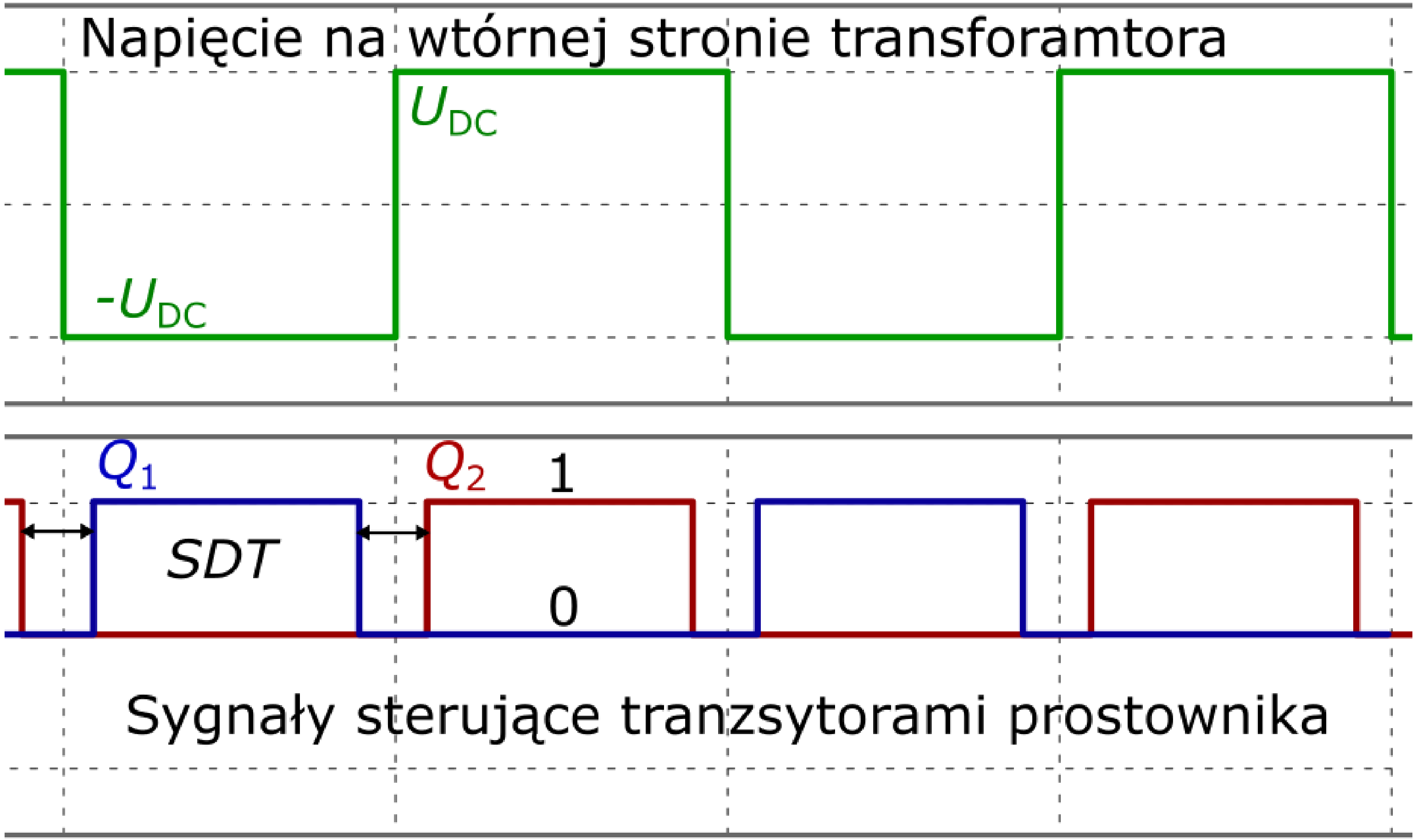
Wyzwania związane z aktywanym prostownikiem

- Brak zintegrowanych układów scalonych dla wysokonapięciowych prostowników aktywnych (> 200 V)
- Sterowanie w otwartej pętli jest niewystarczające ze względu na szeroki zakres napięcia wyjściowego
- Pomiar napięcia na tranzystorze jest złożony i trudny do niezawodnej implementacji

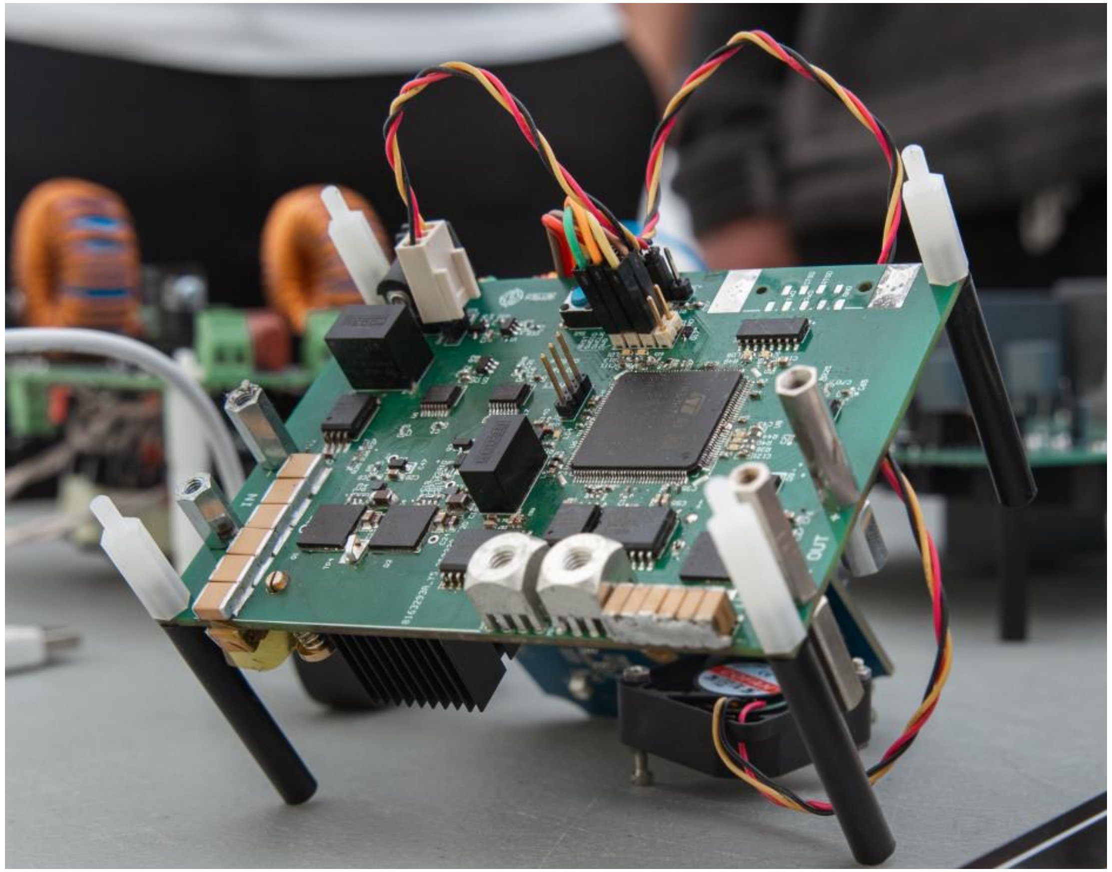
Dedykowana strategia sterowania

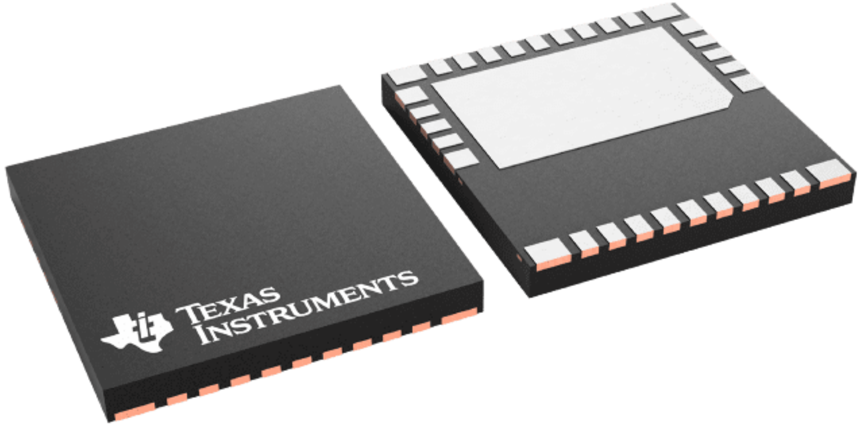
- Analiza SOA (Safe Operating Area) dla momentu załączania prostownika aktywnego
- Zastosowanie LUT opartej na prądzie i napięciu wyjściowym
- Implementacja zabezpieczenia: wyłączanie prostownika przy pracy poza obszarem SOA

Sterowanie prostownika aktywnego



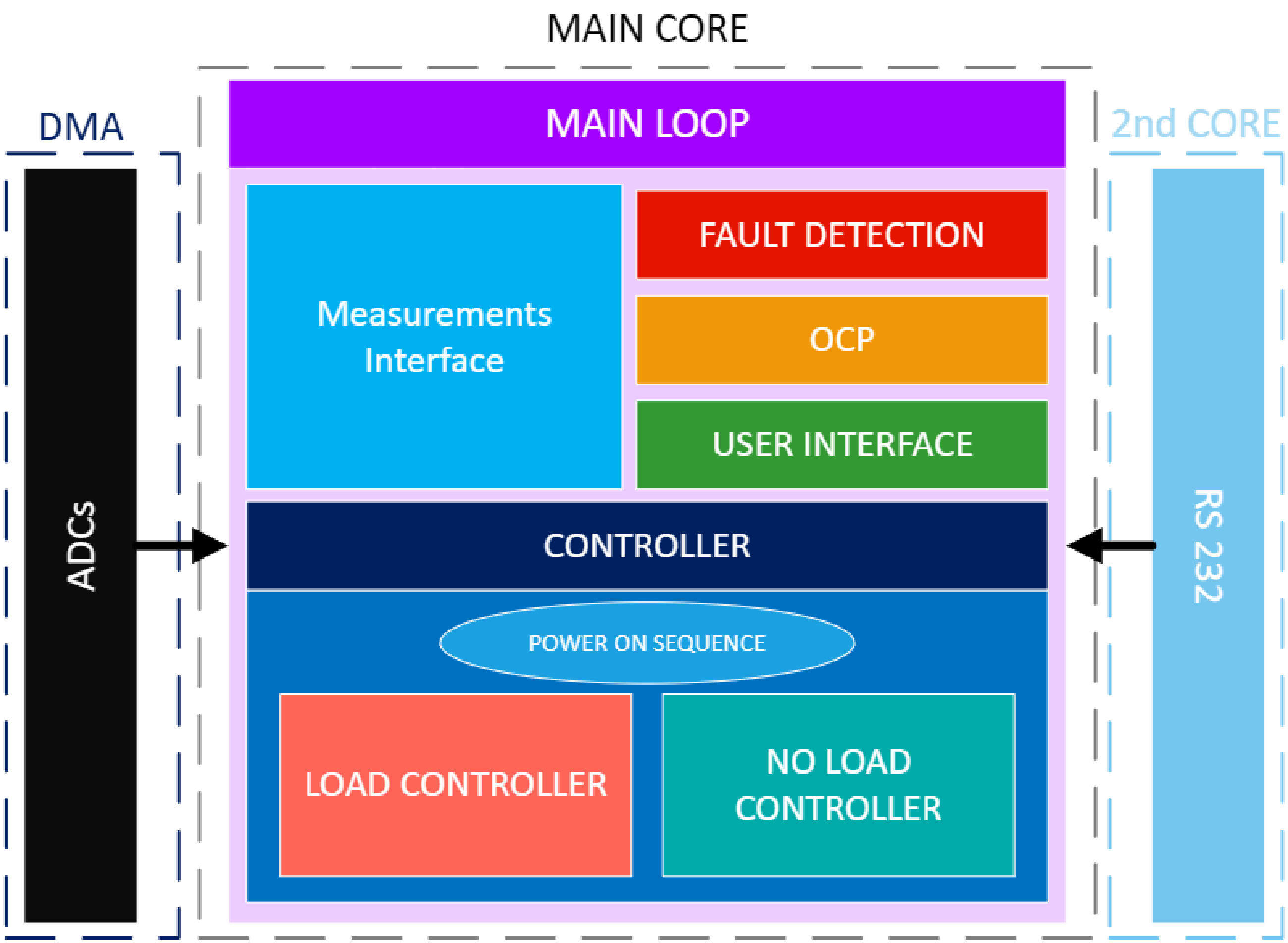
Półprzewodniki



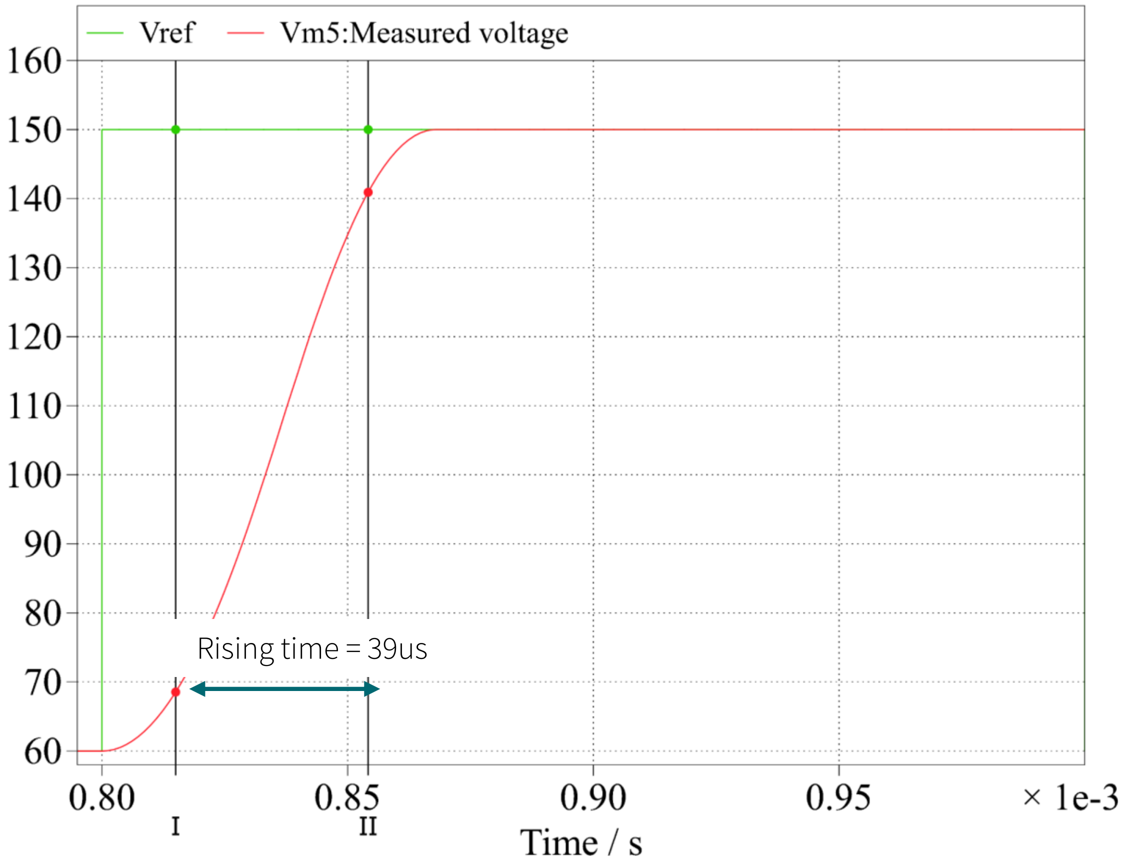


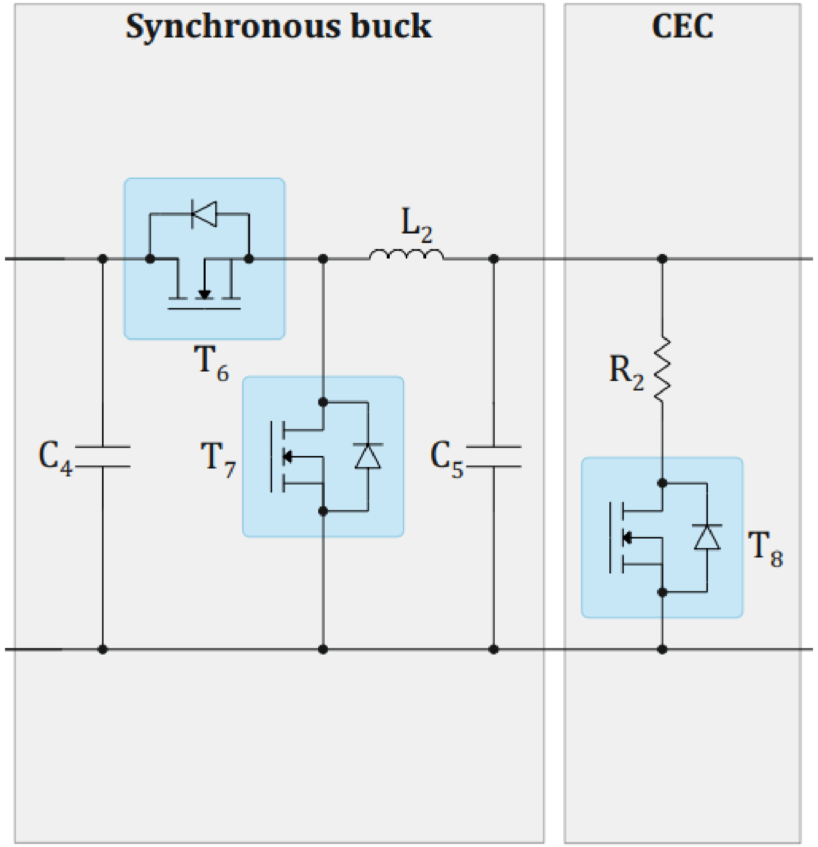
LMG3411R050RWHT

Układ sterowania



Sterowanie w stanach bez obciążenia

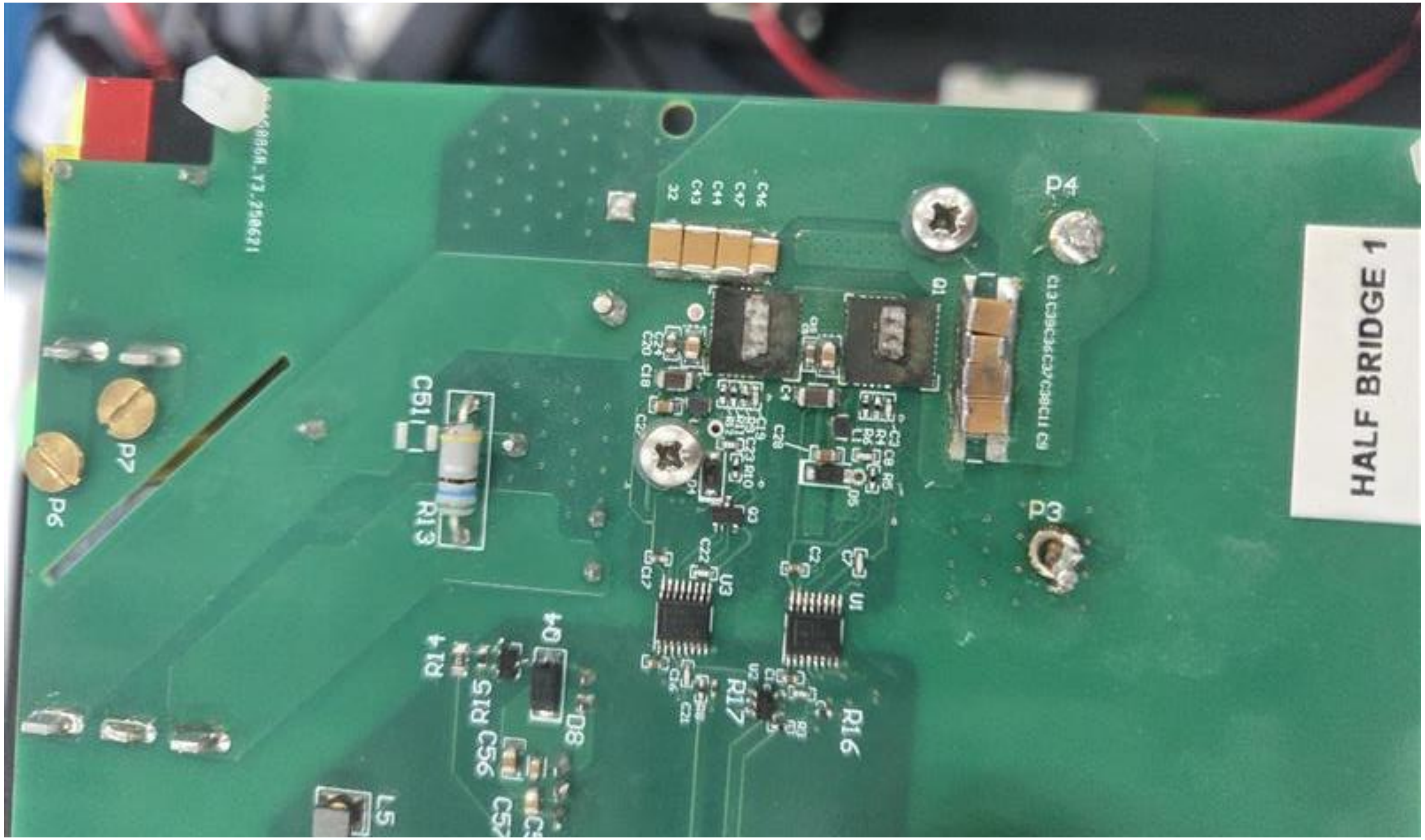

Rising time = 39us



Finał na Tajwanie – Chroma ATE

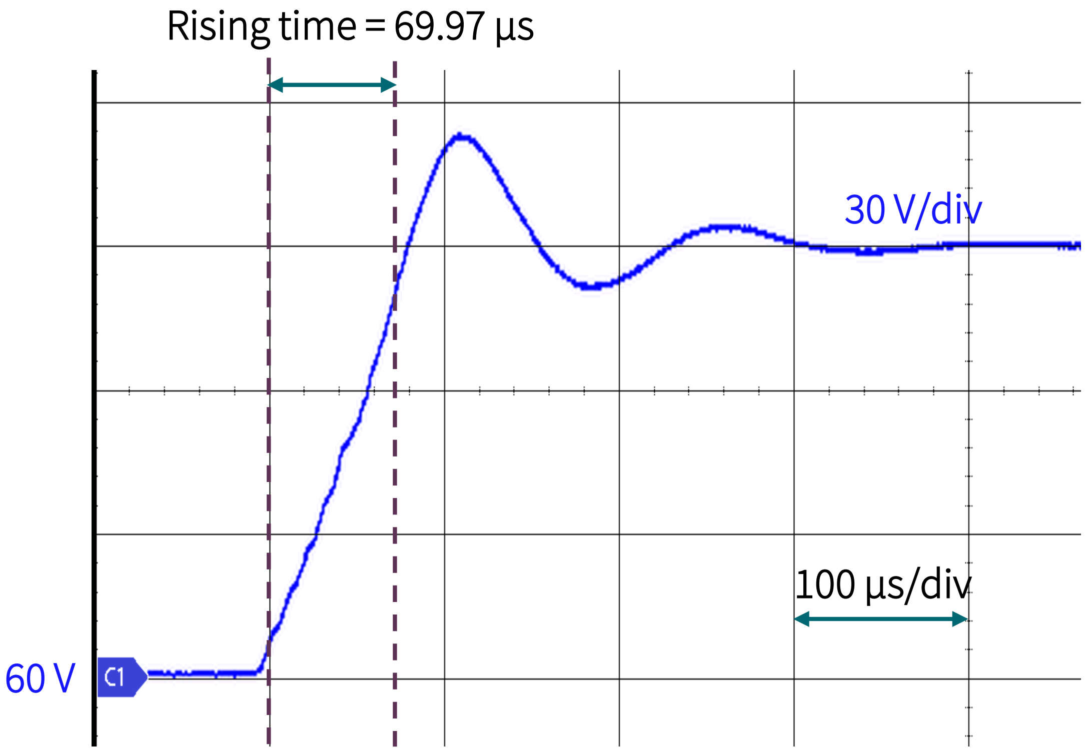
1. Electrical tests
    - Step response of output voltage
    - Dynamic performance
    - Voltage accuracy & load regulation
    - Voltage noise & ripple
    - Conversion efficiency
    - Protection function validation
2. Burn-in test
3. Safety test (Hi-pot test)
4. Physical characteristics and design objectives

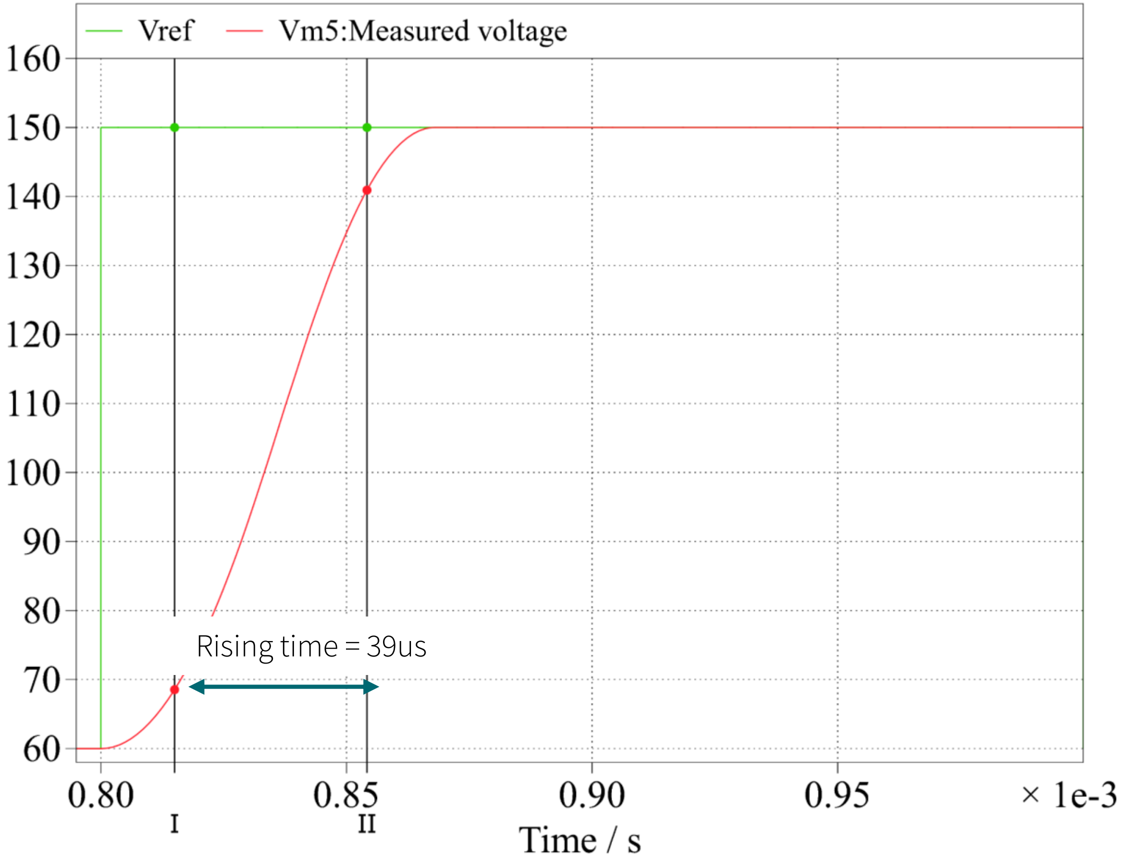
Finał na Tajwanie – falstart



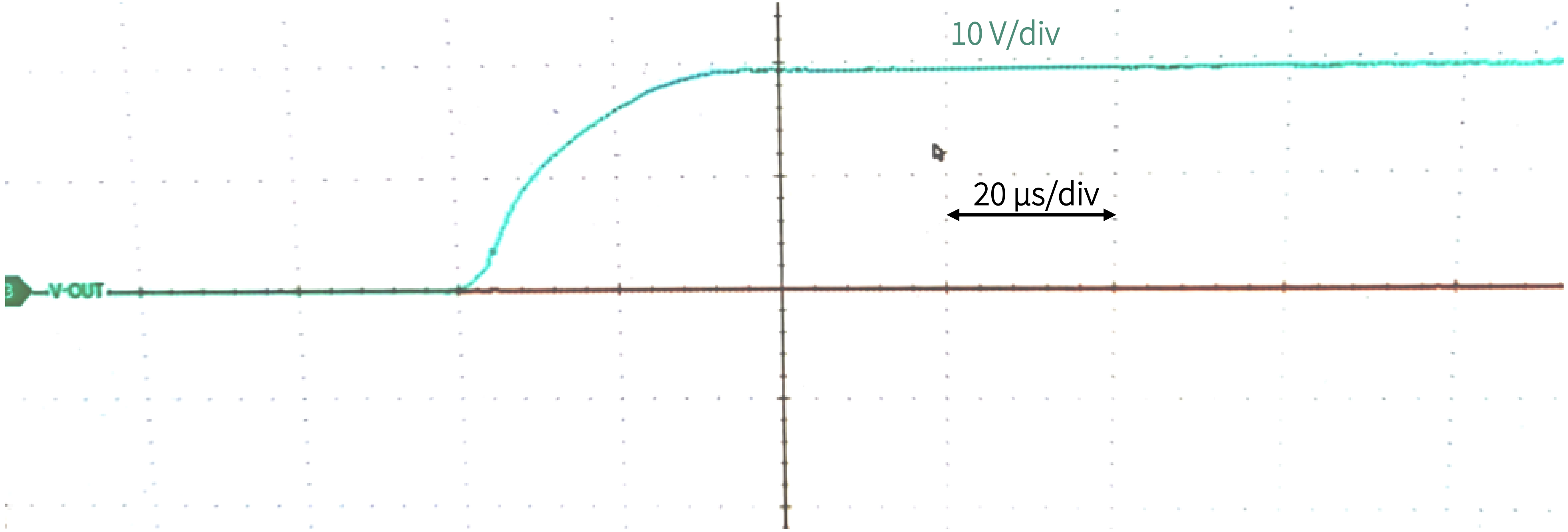
Wyniki pomiarów

Step response of output voltage – 60 V ⟶ 150 V (No load)



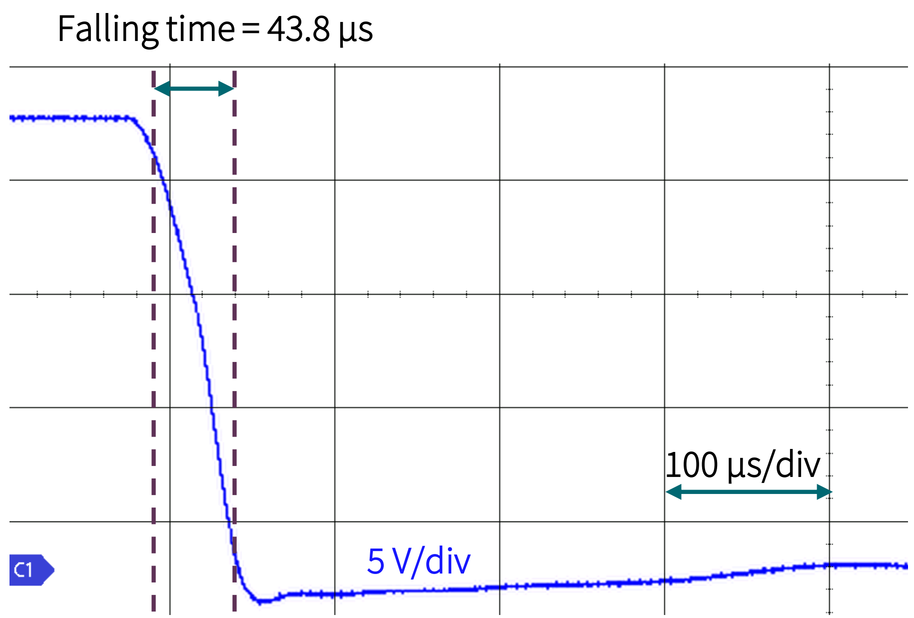


Step response of output voltage – 0 V → 20 V

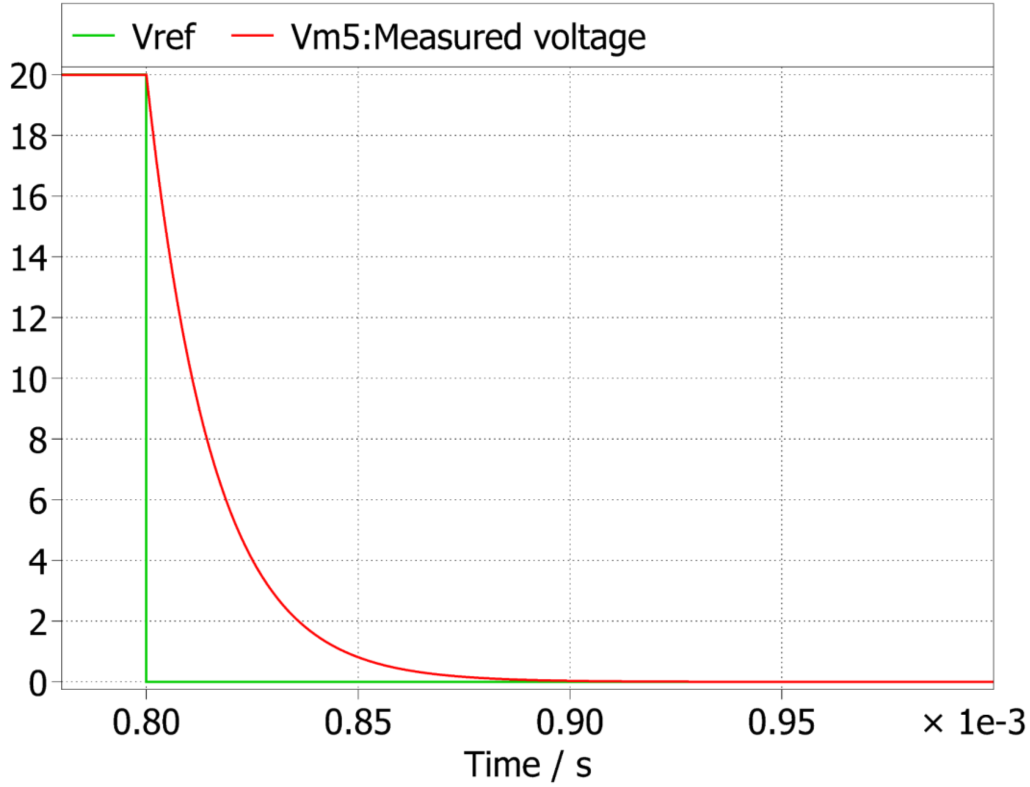


Step response of output voltage – 20 V ⟶ 0 V

Measurement results



Simulation results

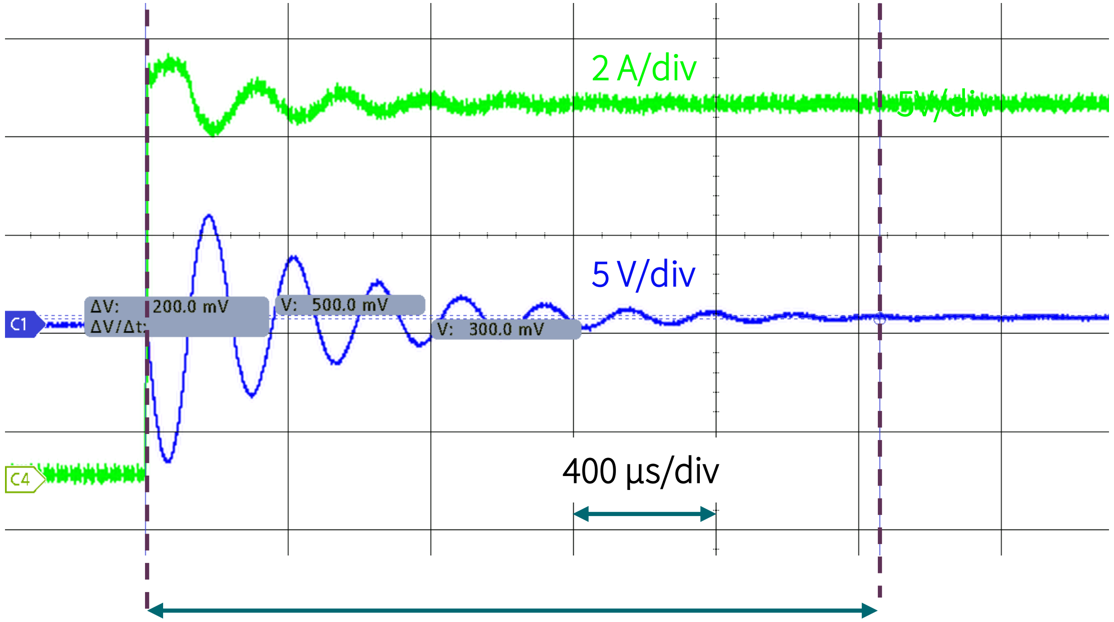


Step response of output voltage

	Dynamic Performance	Specification	Test Result	PASS/FAIL
20 V → 60 V	Rising time	<100us	46.05us	PASS
60 V → 150 V	Rising time	<100us	69.97us	PASS
150 V → 60 V	Falling time	<1ms	0.061ms	PASS
60 V → 20 V	Falling time	<1ms	0.055ms	PASS
20 V → 0 V	Falling time	<1ms	0.044ms	PASS

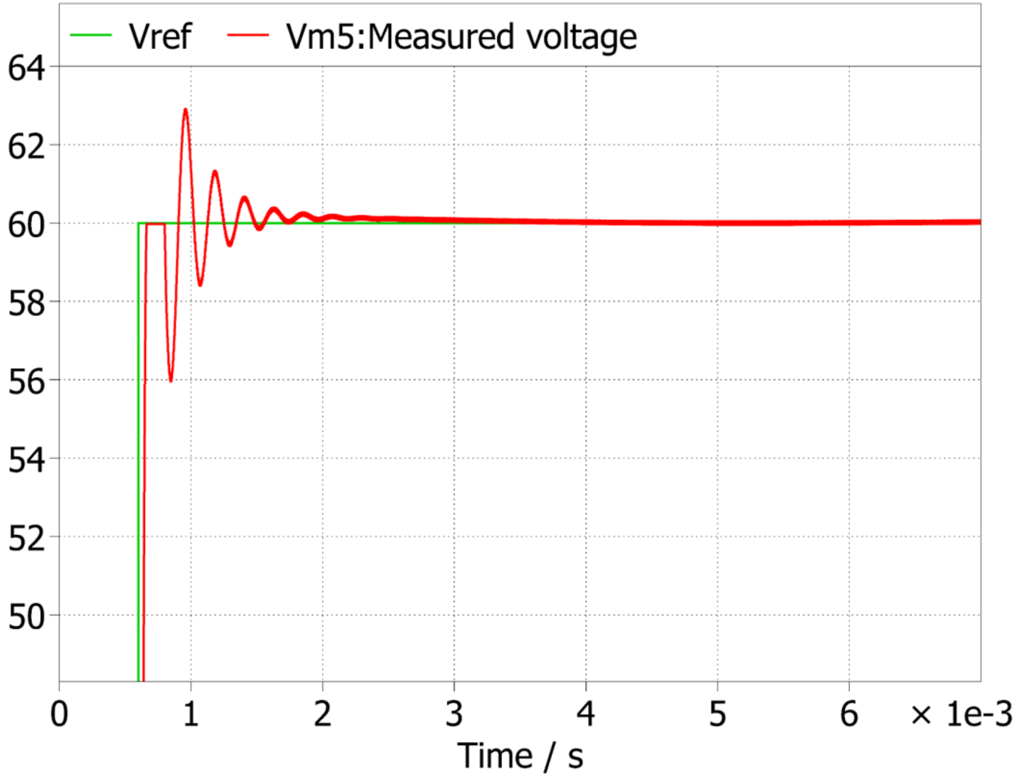
Dynamic performance - load regulation 0 → 10 A

Measurement results



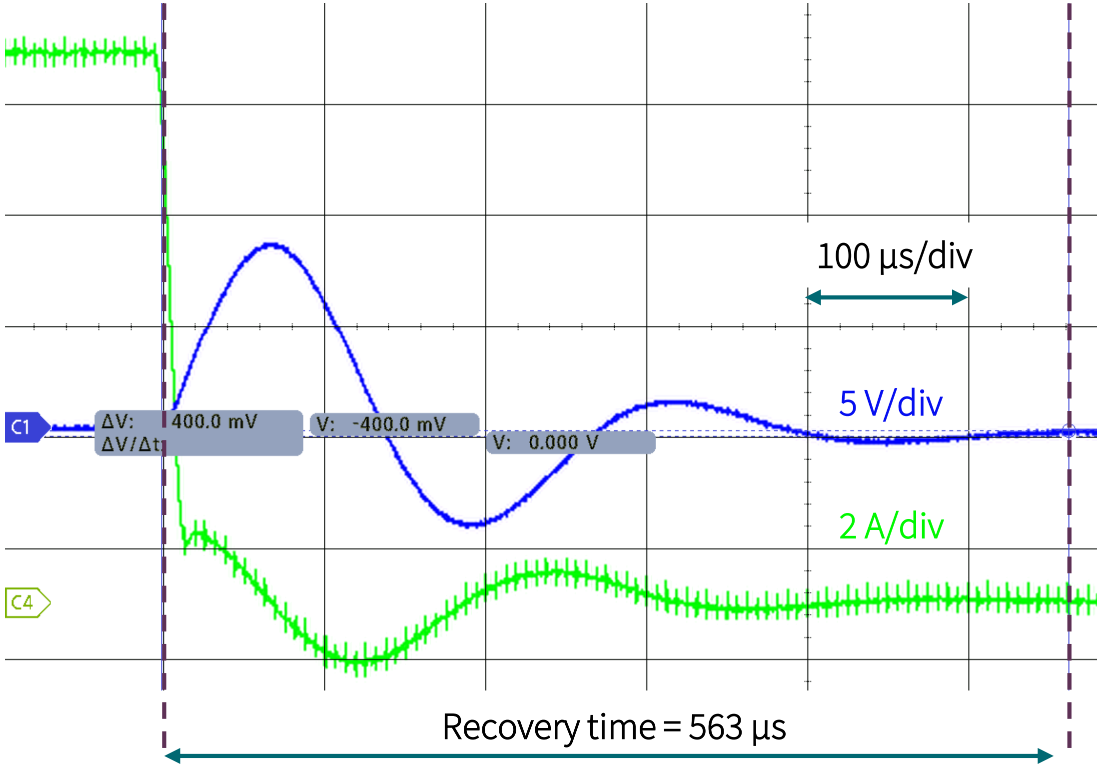
Recovery time = 2.06 ms

Simulation results



Dynamic performance - load regulation 10 → 0 A

Measurement results



100 µs/div

5 V/div

2 A/div

Recovery time = 563 µs

Dynamic performance - load regulation

	Dynamic Performance	Specification	Test Result	PASS/FAIL
20 V, 0 → 10 A	Recovery Time	< 0.1ms	2.06ms	FAIL
20 V, 10 A → 0	Recovery Time	< 0.1ms	0.563ms	FAIL
60 V, 0 → 10 A	Recovery Time	< 0.1ms	1.59ms	FAIL
60 V, 10 A → 0	Recovery Time	< 0.1ms	0.635ms	FAIL
150 V, 0 → 10 A	Recovery Time	< 0.1ms	1.7ms	FAIL
150 V, 10 A → 0	Recovery Time	< 0.1ms	1.712ms	FAIL

Voltage accuracy & load regulation

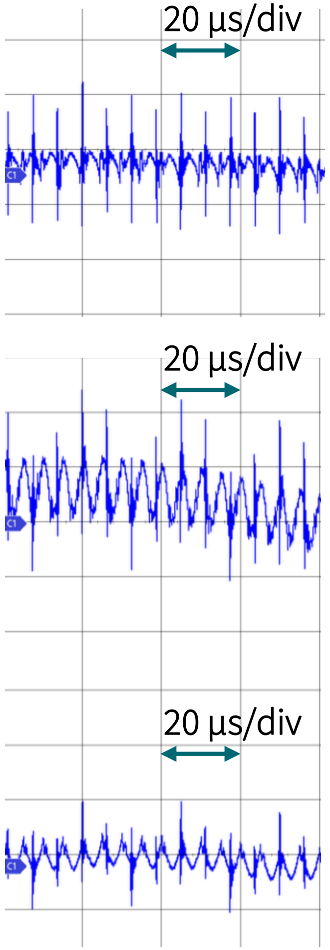
Voltage Accuracy	Specification	Test Result	PASS/FAIL
No Load	< ±0.5%	-0.21% to 0.31%	PASS
Full Load	< 0.1%	-0.06% to 1.42%	FAIL

Load Regulation	Specification	Test Result	PASS/FAIL
20V	< 0.1%	-1.3%	FAIL
60V		0.37%	FAIL
150V		-0.26%	FAIL

Voltage noise

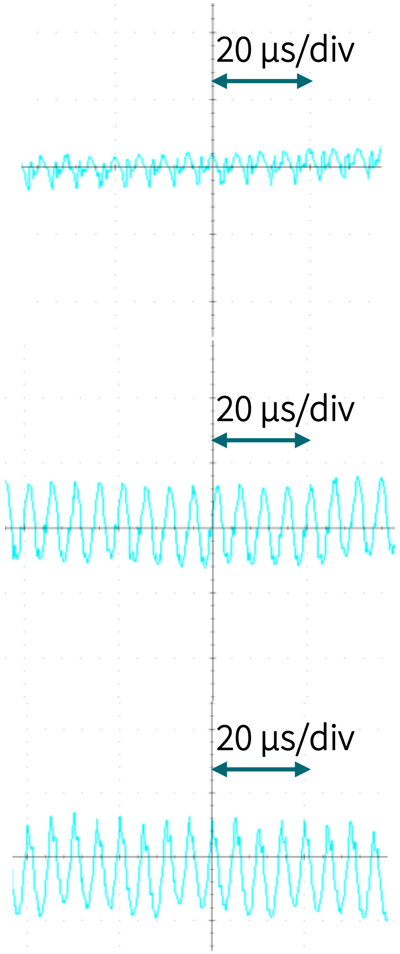
On-site measurement results

Voltage	Test Result
20V	295.9mVp-p
60V	425.5mVp-p
150V	435.1mVp-p



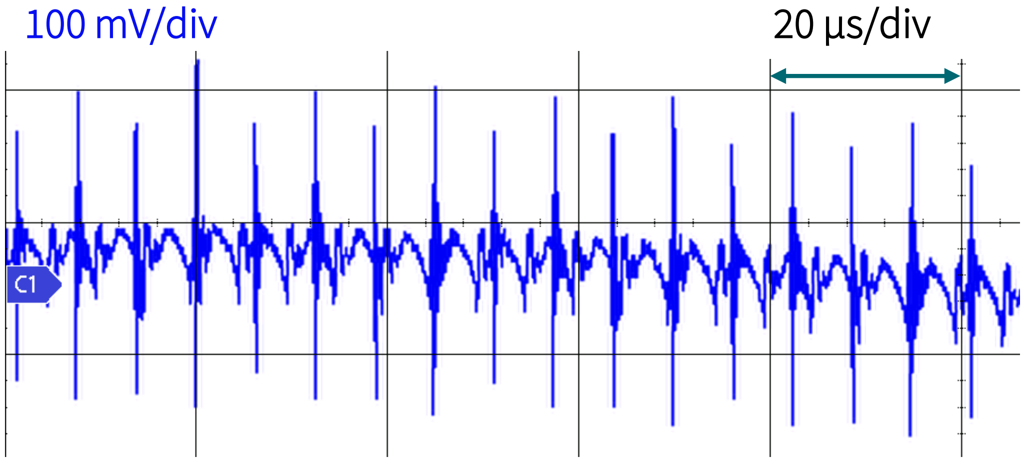
WUT lab results

Voltage	Test Result
20V	73mVp-p
60V	160mVp-p
150V	174mVp-p

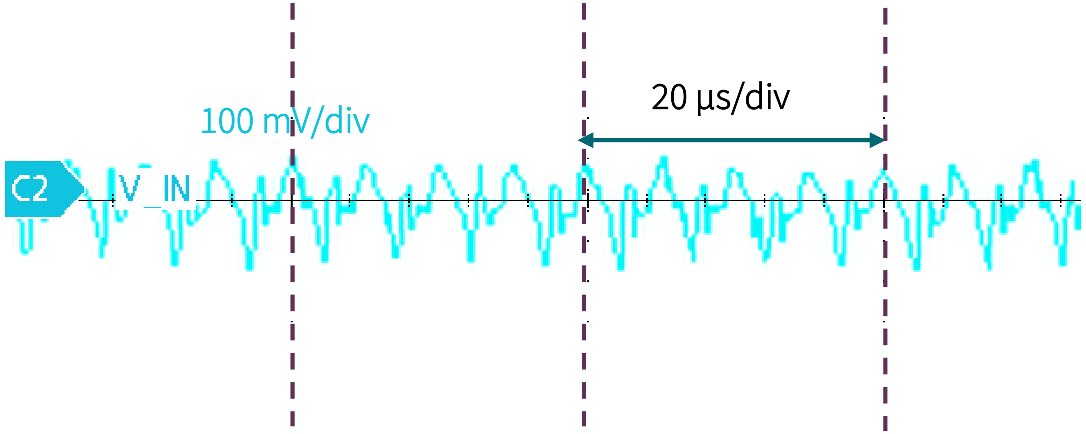


Voltage ripple

IFEC lab results

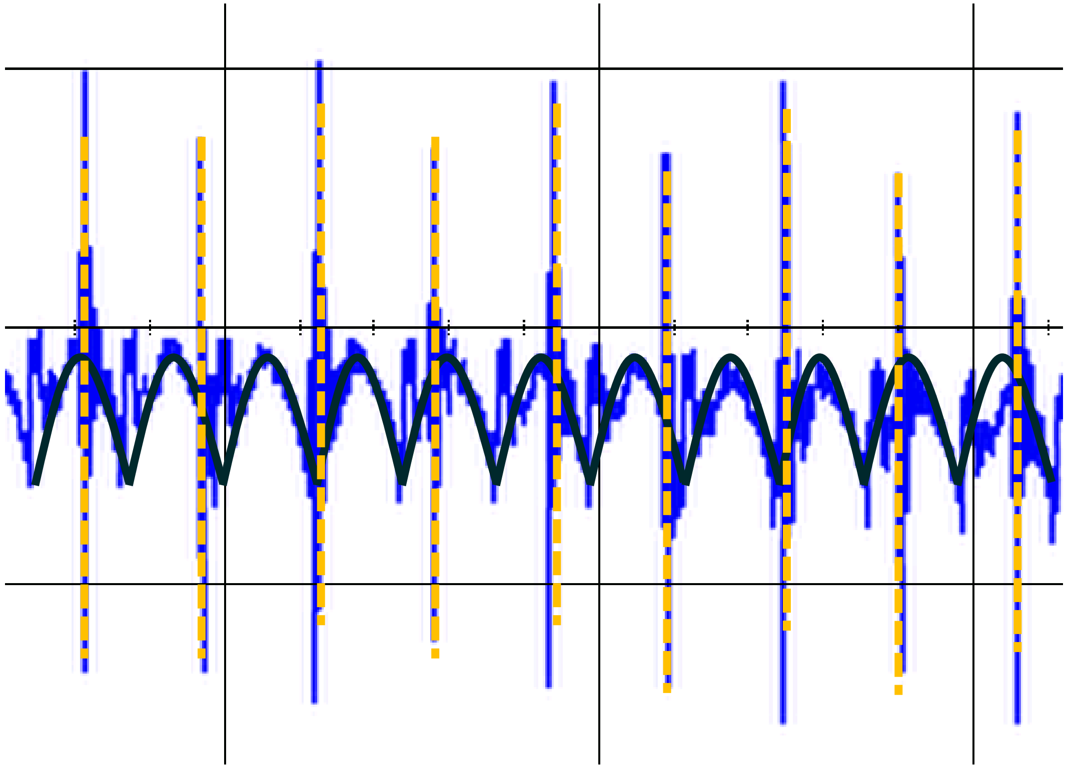


WUT lab results

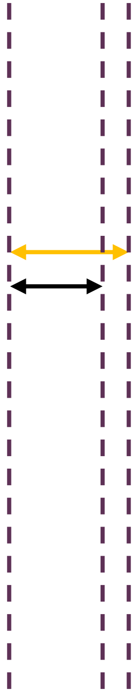


Voltage ripple

Interference on IFEC noises measurements



Not our frequency

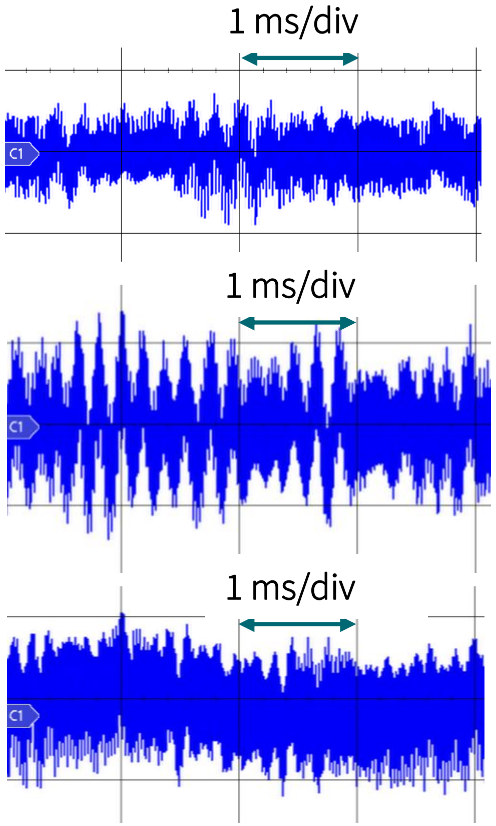


Period difference

Voltage noise

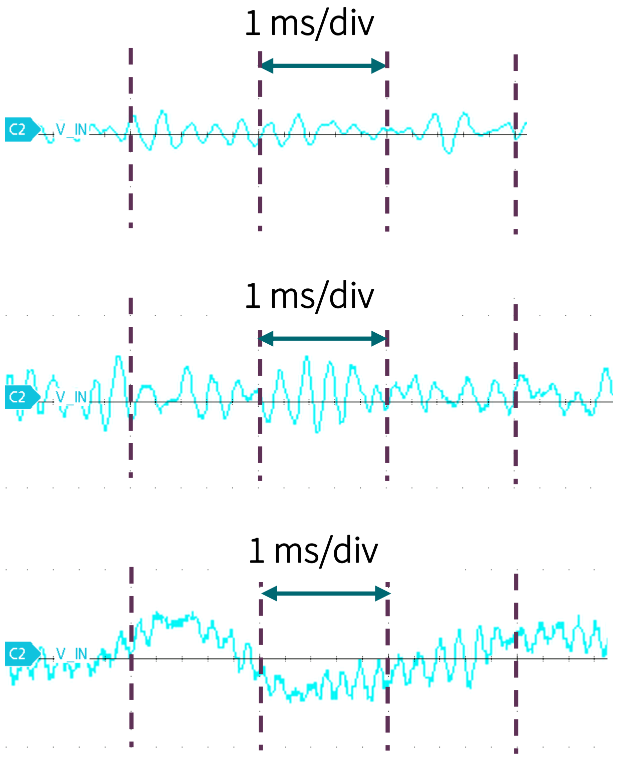
On-site measurement results

Voltage	Test Result
20V	15.95mVrms
60V	38.55mVrms
150V	35.46mVrms



WUT Lab results

Voltage	Test Result
20V	9mVrms
60V	20mVrms
150V	26mVrms

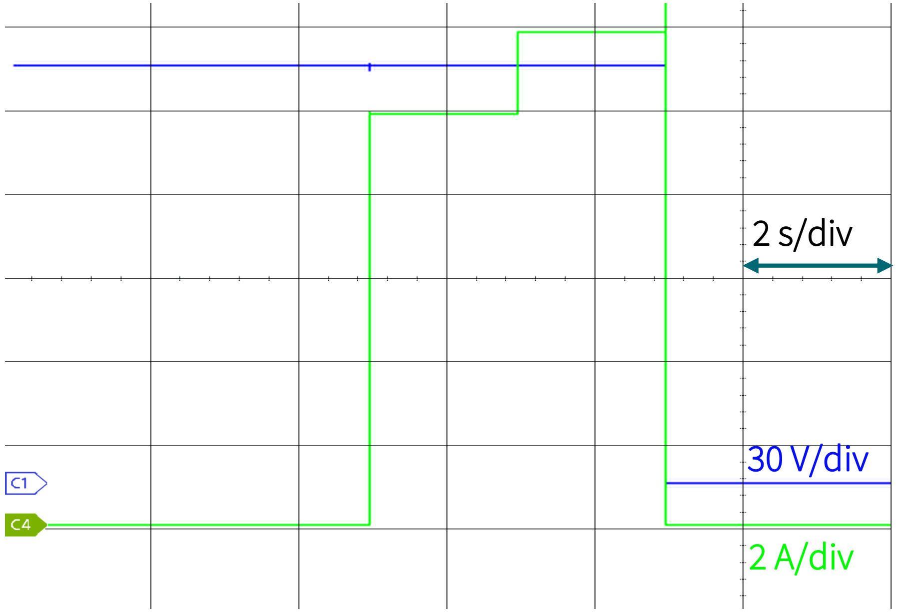


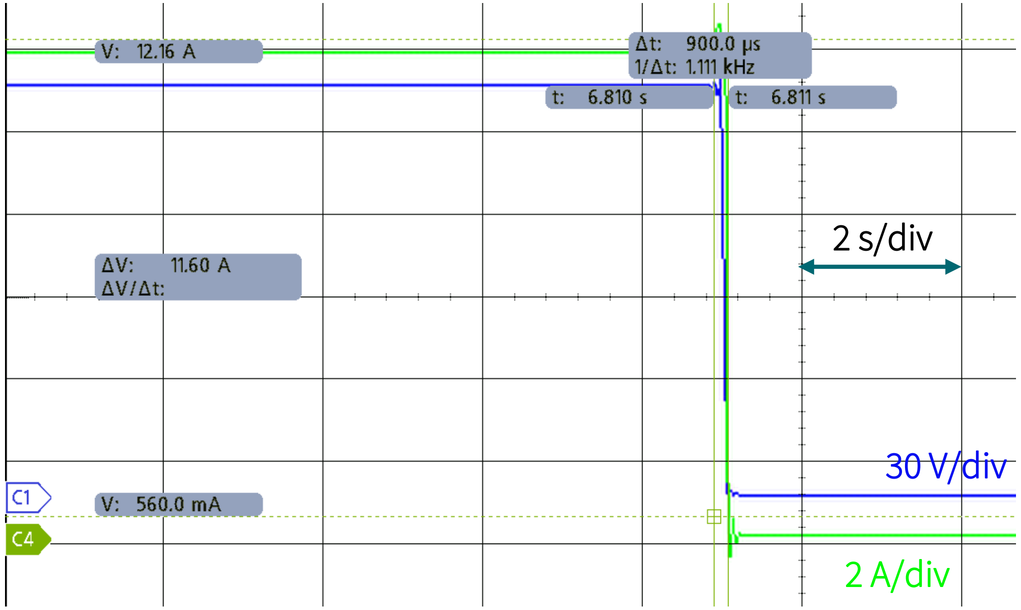
Conversion efficiency

Vo Setting (V)	Load Current Setting (A)	Measurement Output Power Value (W)	Measurement Input Power Value (W)	Conversion Efficiency	Conversion Specification	PASS/FAIL
150	2.5	384.07	400.90	95.80%	> 92%	PASS
	5	762.69	785.33	97.12%	> 96%	PASS
	10	1505.80	1553.90	96.90%	> 95%	PASS

Protection function validation

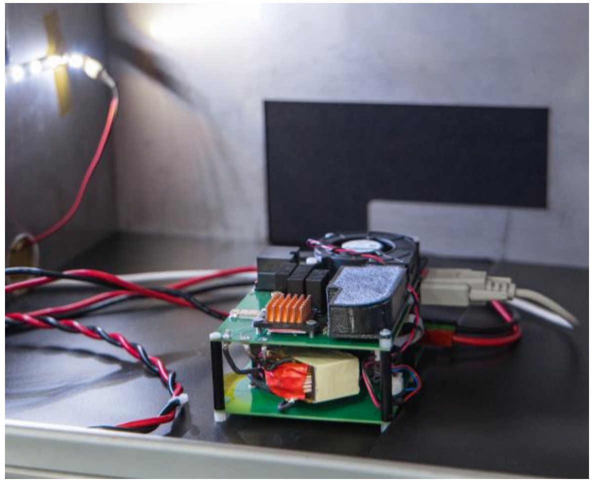
	Pass Criteria	Test Result	PASS/FAIL
Overload Capability	Po = (150V * 12A) ±10%		PASS
OCP Triggered	< 100ms	900µs	
Re-Enable	VDC = 150V ±5%		





Burn-in test

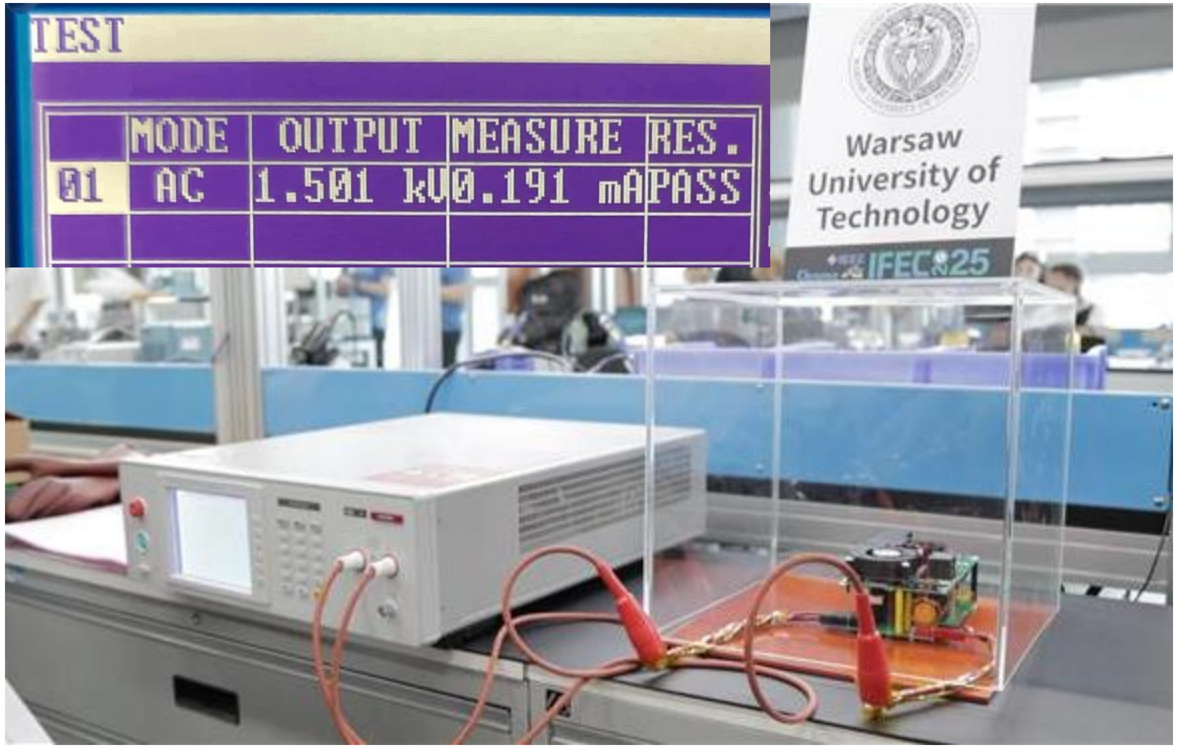
	Load Condition	Pass Criteria	Test Result
Burn-in Test	Full Load	VDC = 150V ±5%, no damage	PASS
	No Load	VDC = 150V ±5%, no damage	PASS



10 min 👍

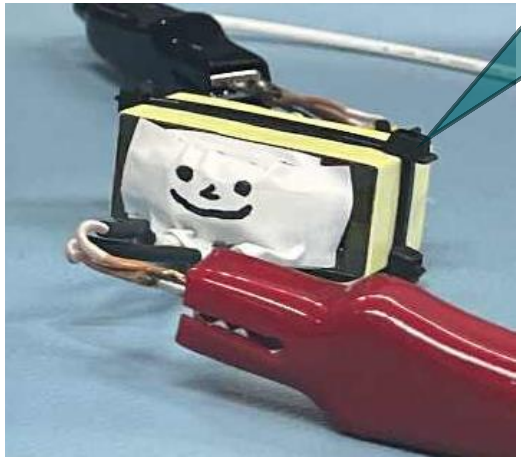
Safety test (Hi-pot test)

	Pass Criteria	Test Result	PASS/FAIL
Leakage Current	< 8mA, no damage	0.191mA	PASS



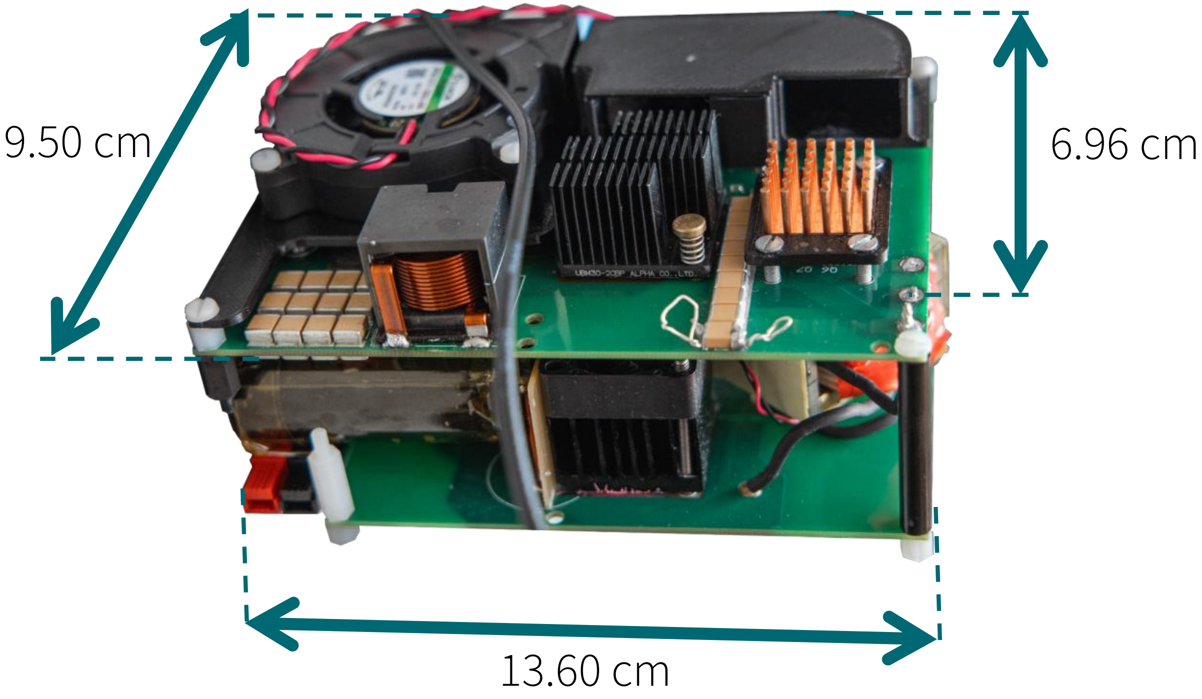
```
TEST
   MODE  OUTPUT    MEASURE  RES.
01  AC   1.501 kV  0.191 mA PASS
```

Lab results



Physical characteristics and design objectives

	Pass Criteria	Test Result	PASS/FAIL
Length	< 30cm	13.60 cm	PASS
Width	< 30cm	9.50 cm	PASS
Height	< 15cm	6.96 cm	PASS
Volume	< 1000 cm^3	898.78 cm^3	PASS
Weight	< 1.5kg	0.585 kg	PASS
Power Density	> 1.6W/cm^3	1.675 W/cm^3	PASS
Weight Density	-	2574.02 W/kg	PASS
Fan noise	< 55dB	32.8dB	PASS



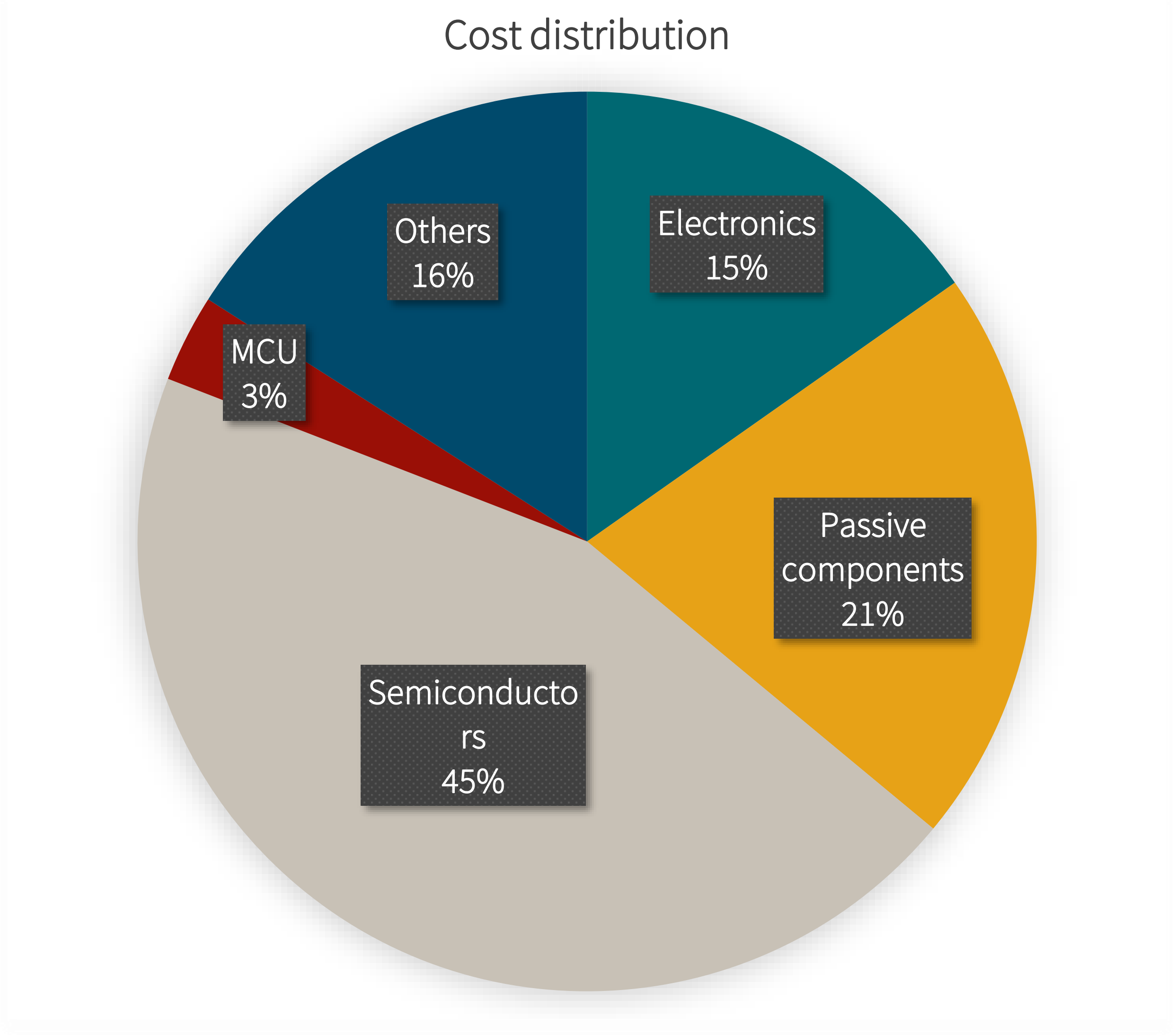
BOM cost breakdown

Cost of 1 unit: **$348.72**

Cost of 1000 units: **$348,720.00**

	Cost of 1 unit
Semiconductors	$156.48
Passive components	$72.44
Others	$55.64
Electronics	$53.16
MCU	$11.00

Prices as of 14 July 2025



Studencki Ruch Naukowy StRuNa

Nagroda Główna w kategorii StRuNa-TECH

gólnopolski konkurs dla autorów i promotorów najlepszych projektów naukowych realizowanych zespołowo przez studentów i doktorantów

KONKURS
StRuNa
2025

KN Drones Renewables
oraz KN Power Electronics
And Plasma Applications

z Politechniki Warszawskiej

zdobyły pierwszą nagrodę
w kategorii

StRuNa-TECH 2025

za innowacyjny izolowany przekształtnik DC-DC
o wysokiej sprawności i szybkiej odpowiedzi dynamicznej

Minister Nauki
i Szkolnictwa Wyższego

Nagroda główna StRuNa-TECH 2025
dla kół naukowych Drones Renewables
oraz Power Electronics And Plasma
Applications z Politechniki Warszawskiej

Dziękuję za uwagę

Hardware Design Masterclasses, 28.11.2025
Paweł Wodzyński

Faculty of Electrical Engineering
Warsaw University of Technology